GigaDevice Semiconductor Inc.

Migration from GD32E5xx to GD32G5xx series

Application Notes
AN218

Revision 1.0

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1. Foreword

The GD32G5xx series of MCUs is based on the ARM® Cortex®-M33 processor and represents a new generation of 32-bit general-purpose microcontrollers. Compared to the GD32E5xx series, the GD32G5xx series has seen significant upgrades in terms of product performance, peripheral resources, and functionality. This article primarily introduces these two series of chips from three aspects: hardware resource comparison, peripheral and performance comparison, and peripheral difference comparison, aiming to help developers quickly migrate from GD32E5xx to GD32G5xx, shorten the R&D cycle, and accelerate product development progress.

Table 1-1. Applicable products

Series	Model number
GD32E5xx	GD32E503/E505/E507/E508
	GD32E513/E515/E517/E518
GD32G5xx	GD32G533/G553

2. Hardware resource comparison

The hardware pin comparison between GD32G5xx and GD32E5xx, taking LQFP64 as an example, is shown in *Figure 2-1 GD32G5xx and GD32E5xx pin comparison*. From this figure, it can be seen that the pin definitions of GD32G5xx are different from those of GD32E5xx. If replacement is needed, users will need to redesign the hardware.

Figure 2-1. GD32G5xx and GD32E5xx pin comparison

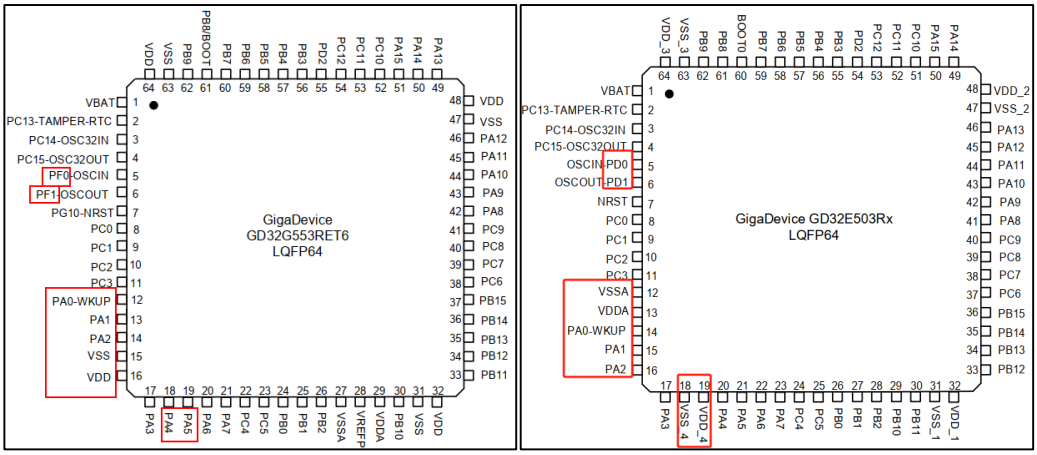

Table 2-1 Packaging types and compatibility of GD32G5xx and GD32E5xx presenting the different packaging options for the two chips and the differences among them.

Table 2-1. Packaging types and compatibility of GD32G5xx and GD32E5xx

Packaging types	GD32G5xx	GD32E5xx	Compatibility
QFN48	√	√	Incompatible
LQFP48	√	√	Incompatible
LQFP64	√	√	Incompatible
WLCSP81	√		—
LQFP100		√	Incompatible
LQFP128	√		—
LQFP144		√	—

Note: “ √ ” indicates the presence of that type of packaging, “—” indicates no need for it.

3. Peripheral and Performance comparison

The GD32G5xx has a richer set of peripheral resources, which can cover the commonly used peripheral resources of the GD32E5xx. The specific system and peripheral resource comparison is shown in ***Table 3-1 System and peripheral resource comparison between GD32G5xx and GD32E5xx***.

Table 3-1. System and peripheral resource comparison between GD32G5xx and GD32E5xx

System and peripheral resource	GD32G5xx	GD32E5xx	Remark
Clock frequency	216MHz	180MHz	
Core	M33 (without trustzone)	M33 (without trustzone)	
Flash	Up to 512KB dual bank	Up to 512KB single bank	Incompatible
SRAM	Entire series 128KB	96/128KB	Incompatible
Power supply range	1.71V-3.6V	1.71V-3.6V	
Temperature Range	-40℃~85℃/-40℃~105℃	-40℃~85℃/-40℃~105℃	
Timer	Advanced timer *3 (16bit)	Advanced timer *2 (16bit)	Compatible
	GP timer *7 (16bit *5 + 32bit *2)	GP timer *10 (16bit *9 + 32bit *1)	Compatible
	Basic timer *2 (16bit)	Basic timer *2 (16bit)	Compatible
	High-Precision Timer *1 (Maximum resolution 144ps)	High-Precision Timer *1 (Maximum resolution 86.8ps)	Partially compatible
	Low-Power Timer *1	—	
U(S)ART	USART*3 + UART*2	USART*4 + UART*2	Compatible
HRTIMER	1 Master_Timer+ 8 Slave_Timer	1 Master_Timer+ 5 Slave_Timer	Compatible
IIC	4	3	Partially compatible
SPI	3	3	Compatible
SQPI	—	1	
QSPI	1	—	Functionality can cover E5 SQPI
CAN	FD *3	FD *3	Incompatible
USB	—	USBFS+USBHS (Internal PHY)	
SDIO	—	1	
Ethernet	—	1	
EXMC	1	1	Partially compatible

ADC	4 units with 42 external channels + 11 internal channels	3 units with 21 external channels + 2 internal channels	Partially compatible
DAC channels	4	2	Partially compatible
CAU	1	—	
TRIGSEL	1	—	
CLA	1	—	
TRNG	1	—	
TMU	1	1	Compatible
VREF	1	—	
HDPF	1	—	
FAC	1	—	
FFT	1	—	
CMP	8	3	Compatible
GPIO	107	112	

4. Differences of peripheral devices

4.1. On-chip SRAM

The maximum SRAM capacity for both GD32G5xx and GD32E5xx is 128KB, but there are differences in the address distribution. For specific details, refer to ***Table 4-1 SRAM distribution of GD32G5xx and GD32E5xx***.

Table 4-1. SRAM distribution of GD32G5xx and GD32E5xx

SRAM type	GD32G5xx	GD32E5xx
SRAM0	0x2000 0000 – 0x2001 3FFF (80KB)	0x2000 0000 - 0x2001FFFF (128KB)
SRAM1	0x2000 4000 – 0x2001 7FFF (16KB)	—
TCMSRAM	0x1000 0000 – 0x1000 7FFF (32KB)	—

Additionally, the SRAM in GD32G5xx features ECC functionality, supporting 1-bit error correction and multi-bit error detection, while the SRAM in GD32E5xx does not include ECC functionality.

4.2. FMC

The maximum Flash size for both GD32G5xx and GD32E5xx is 512KB. The difference is that E5xx has a single Bank with a flash page size of 8KB; whereas G5xx can be configured for single/double Bank operation. In single Bank mode, the flash page size is 1KB, which means that the code running in another Bank will not be blocked while erasing or writing Flash. In double Bank mode, the flash page size is 2KB. For specific details, refer to ***Table 4-2 Flash address distribution of GD32G5xx and GD32E5xx***.

Table 4-2. Flash address distribution of GD32G5xx and GD32E5xx

SRAM type	GD32G5xx	GD32E5xx
SRAM0	0x2000 0000 – 0x2001 3FFF (80KB)	0x2000 0000 - 0x2001FFFF (128KB)
SRAM1	0x2000 4000 – 0x2001 7FFF (16KB)	—
TCMSRAM	0x1000 0000 – 0x1000 7FFF (32KB)	—

4.3. AFIO

The AF capabilities of the I/O ports on GD32E5xx are relatively fixed, whereas on GD32G5xx, the AF capabilities of the I/O ports are selected through AF numbers, which reduces the likelihood of conflicts between I/O ports.

4.4. DMA and DMAMUX

GD32E5xx is equipped with two DMA controllers, where DMA0 has 7 channels and DMA1 has 5 channels, with each DMA channel being tied to specific peripheral trigger conditions. In contrast, GD32G5xx also has two DMA controllers, with DMA0 having 7 channels and DMA1 having 7 channels. Additionally, GD32G5xx introduces a DMAMUX, which enables any DMA channel to select any peripheral trigger condition, greatly increasing the flexibility of the DMA system.

4.5. TMU trigonometric function accelerator

GD32E5xx has a TMU with 9 modes, and it only supports the IEEE-754 32-bit single-precision floating-point format for operational data. GD32G5xx, on the other hand, has a TMU with 10 modes (supporting more complex operations), and it supports both q1.31 and q1.15 fixed-point formats as well as the IEEE754 32-bit single-precision floating-point format for operational data.

4.6. ADC

The differences in the ADC between the two chips are detailed in ***Table 4-3 ADC differences between GD32G5xx and GD32E5xx***.

Table 4-3. ADC differences between GD32G5xx and GD32E5xx

ADC differences	GD32G5xx	GD32E5xx
Number of ADC	4	3
Number of channels ADC	ADC0：14 external+5 internal ADC1：16 external +3 internal ADC2：15 external +5 internal ADC3：18 external +3 internal	ADC0：16 external +2 internal ADC1：16 external ADC2：13 external
Number of IOs available for ADC	42	21
External trigger sources for ADC	Configured with TRIGSEL with greater flexibility	ADC has a fixed number of trigger sources, which is quite restrictive
Reference source	External voltage reference source or internal reference source	External voltage reference source
Internal channels	Temperature sensor High-precision temperature sensor Vrefint	Temperature sensor Vrefint

	Battery voltage detection channel DAC_OUT channel	
ADC synchronization	Supports synchronization of two ADCs (ADC0 and ADC1) or three ADCs (ADC0, 1, 2)	Only supports synchronization of ADC0 and ADC1

4.7. DAC

The differences in DAC between the two chips are shown in ***Table 4-4 DAC differences between GD32G5xx and GD32E5xx***.

Table 4-4. DAC differences between GD32G5xx and GD32E5xx

DAC difference items	GD32G5xx	GD32E5xx
Number of DAC	4	1
Number of DAC channels	DAC0：2 external DAC1：2 external DAC2：2 internal DAC3：2 internal	DAC：2 external
Number of IOs available for DAC	4	2
External trigger sources for DAC	Configured with TRIGSEL with greater flexibility	The DAC has a fixed number of trigger sources, which is quite restrictive
Reference source	External voltage reference source or internal reference source	External voltage reference source
Internal channels	Temperature sensor High-precision temperature sensor Vrefint Battery voltage detection channel DAC_OUT channel	Temperature sensor Vrefint
ADC synchronization	Supports synchronization of two ADCs (ADC0 and ADC1) or three ADCs (ADC0, 1, 2)	Only supports synchronization of ADC0 and ADC1

4.8. IIC

The GD32E5xx features 3 IIC interfaces, and the GD32G5xx has 4 IIC interfaces. Specifically, the GD32E5xx is categorized into two types of IIC, with IIC0 and IIC1 being Type I, and IIC2 being Type II; all 4 IIC interfaces of the GD32G5xx are Type II.

4.9. SPI

The GD32E5xx series SPI supports 8-bit or 16-bit data frame formats, and the GD32G5xx SPI supports data frame formats from 4 to 16 bits.

4.10. EXMC

The GD32E5xx EXMC supports access to external media such as: SRAM, ROM, NOR Flash, NAND Flash, PC cards; the GD32G5xx supports: SRAM, ROM, NOR Flash, PSRAM.

4.11. HRTIMER

The differences in HRTIMER between the two chips are shown in ***Table 4-5 Differences in HRTIMER between GD32G5xx and GD32E5xx***.

Table 4-5. Differences in HRTIMER between GD32G5xx and GD32E5xx

HRTIMER difference items	GD32G5xx	GD32E5xx
Number of Slave_Timer	8	5
Number of channels	Up to 16 channels or up to 8 complementary pairs.	Up to 10 channels or up to 5 complementary pairs.
$f_{HRTIMER\_PSCCK}$	Maximum：f_{clk}*64/2 = 216M*64/2=6.912G	Maximum：f_{clk} *64 = 180M*64=11.52G

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial release	Jun.8, 2024

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