GigaDevice Semiconductor Inc.

GD32E5xx Hardware Development Guide

Application Note
AN078

Revision 1.2

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1. Introduction

The article is specially provided for developers of 32-bit general-purpose MCU GD32E5xx series based on Arm® Cortex®-M33 architecture. It provides an overall introduction to the hardware development of GD32E5xx series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this application notes is to allow developers to quickly get started and use GD32E5xx series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32E5xx series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32E5xx series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32E5xx series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32E5xx series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32E5xx series.
6. Reference circuit and PCB Layout design, mainly introduces GD32E5xx series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32E5xx series.

This document also satisfies the minimum system hardware resources used in application development based on GD32E5xx series products.

Table 1-1. Applicable Products

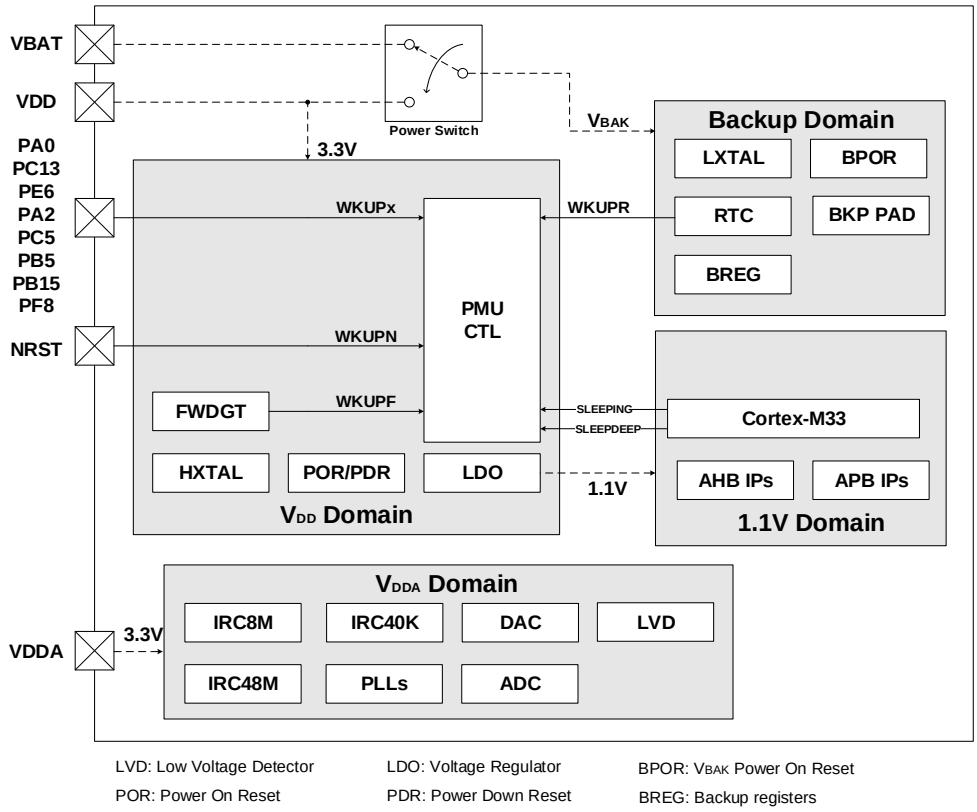
Type	Part Numbers
MCU	GD32E503xx series
	GD32E505xx series
	GD32E507xx series
	GD32E508xx series
	GD32E513xx series
	GD32E517xx series
	GD32E518xx series

2. Hardware design

2.1. Power supply

The V_{DD} / V_{DDA} operating voltage range of GD32E5xx series products is 1.71 V ~ 3.6 V. For GD32E5xx series, there are three power domains, including V_{DD} / V_{DDA} domain, 1.1V domain, and Backup domain, as is shown in ***Figure 2-1. GD32E5xx Power supply overview***.The V_{DD}/V_{DDA} domain is powered directly by the power supply, and an LDO is embedded in the V_{DD}/V_{DDA} domain to power the 1.1 V domain. The backup domain power supply V_{BAK} can be powered by V_{DD} or V_{BAT} through the power switch Power Switch. When the V_{DD} power supply is turned off, the power switch can switch the power supply of the backup domain to the V_{BAT} pin. At this time, the backup domain is powered by the V_{BAT} pin (battery).

Figure 2-1. GD32E5xx Power supply overview



2.1.1. Backup domain

The backup domain supply voltage range is 1.71V ~ 3.6V. In order to ensure the content of the Backup domain registers and the RTC supply, when V_{DD} supply is shut down, V_{BAT} pin can be connected to an optional standby voltage supplied by a battery or by another source. The power switch is controlled by the Power Down Reset circuit in the V_{DD} / V_{DDA} domain.If there is no external battery-powered application, it is recommended to connect the V_{BAT} pin to the ground through a 100nF capacitor and then connect it to the V_{DD} pin.

Note: If the V_{BAT} pin is left floating, the Power Switch will switch V_{BAK} to V_{DD} after the MCU is powered on, and the internal V_{DD} will directly supply power to the Backup domain.

2.1.2. V_{DD}/V_{DDA} domain

The V_{DD} / V_{DDA} power domain supplies power to all areas except the backup domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between the two is required to be less than 300mV (the internal V_{DDA} and V_{DD} are connected by back-to-back diodes). To avoid noise, V_{DDA} can be connected to V_{DD} through an external filter circuit, and the corresponding V_{SSA} can be connected to V_{SS} through a specific circuit (single-point grounding, through 0Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of the ADC, the independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. There is a V_{REFP} and V_{REFN} pin (1.71 V≤V_{REFP}≤V_{DDA}, V_{REFN} = V_{SSA}) for ADC independent power supply on the large package.

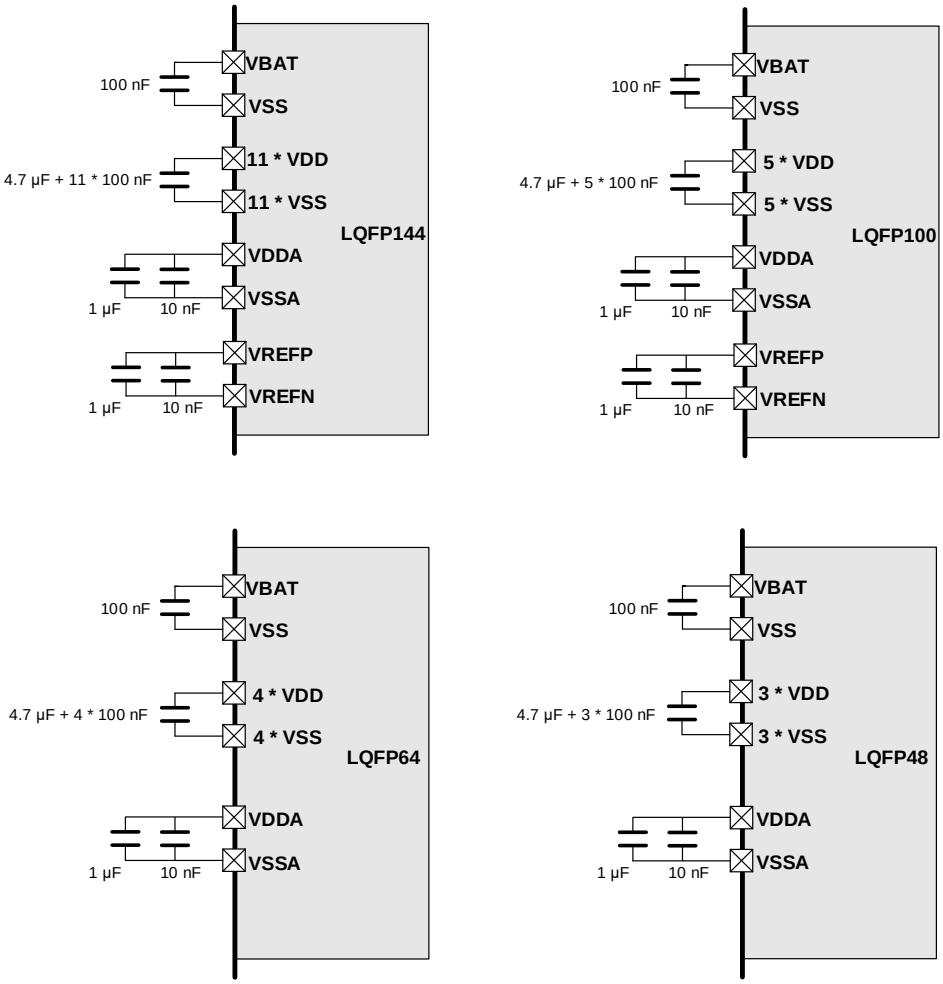
- The package chips with 100 pins and more contain V_{REFP} and V_{REFN}. V_{REFP} can use an external reference power supply, or can be directly connected to V_{DDA}, and V_{REFN} must be connected to V_{SSA}.
- The 64-pin package chip has no V_{REFP} and V_{REFN}, it is directly connected to V_{DDA} and V_{SSA} internally, and all analog modules are powered by V_{DDA} (including ADC/DAC)

2.1.3. Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- The VDD pin must be connected with an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one VDD needs to be connected to GND with a capacitor of not less than 4.7uF, and other VDD pins are connected to 100nF).
- The VDDA pin must be connected with an external capacitor (10nF+1uF ceramic capacitor is recommended).
- The VBAT pin must be connected to an external battery (1.71V ~ 3.6V). If there is no external battery, it is recommended to connect the VBAT pin to the ground through a 100nF capacitor and then connect it to the VDD pin.
- VREFP pin can be directly connected to VDDA. If a separate external reference voltage is used on VREF (2.6V ≤ VREFP ≤ VDDA, VREFN = VSSA), a 10nF+1uF ceramic capacitor must also be connected to ground on the VREFP pin.

Figure 2-2. GD32E5xx Recommended Power Supply Design



Note:

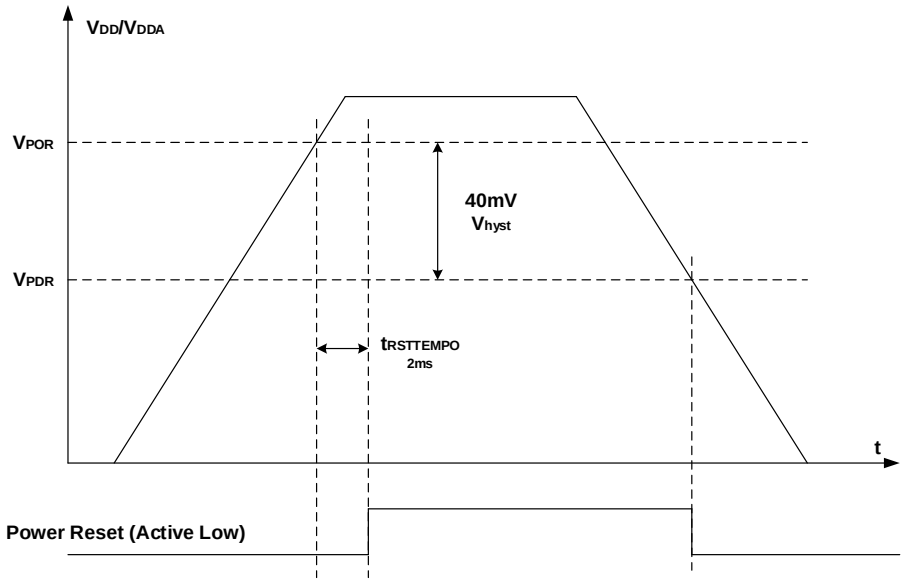
1. All decoupling capacitors must be placed close to the corresponding V_{DD}, V_{DDA}, V_{REFP}, V_{BAT} pins of the chip;
2. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF;
3. V_{BAT} can be directly connected to V_{DD}, or it can be connected to an external battery according to the actual application;
4. LQFP64, LQFP48: VREFP and VDDA are connected internally, VSSA and VREFN are connected internally.

2.1.4. Reset and power management

GD32E5xx series reset control includes three resets: power reset, system reset and backup domain reset. A power reset is a cold reset, which resets all systems except the backup domain when the power is turned on. During the power and system reset process, NRST will maintain a low level until the reset is over. When the MCU cannot be executed, the NRST pin waveform can be monitored by an oscilloscope to determine whether the chip has been reset.

The chip integrates a POR/PDR (power-on/power-down reset) circuit to detect V_{DD}/V_{DDA} and generate a power reset signal to reset the entire chip except the backup domain when the voltage is lower than a certain threshold. V_{POR} represents the threshold voltage of power-on reset, the typical value is about 1.56V, V_{PDR} represents the threshold voltage of power-down reset, and the typical value is about 1.52V. The value of the hysteresis voltage V_{hyst} is about 400mV.

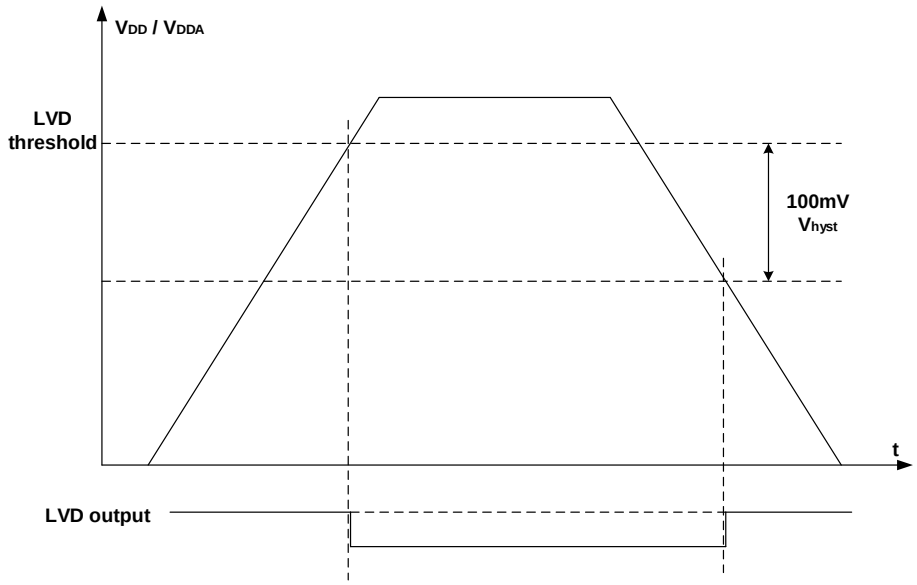
Figure 2-3. Power-on/power-down reset waveforms



The function of LVD is to detect whether the V_{DD}/V_{DDA} supply voltage is lower than the low voltage detection threshold (2.2 V ~ 2.9 V), which is configured by the LVDT[2:0] bits in the power control register (PMU_CTL0). LVD is enabled by setting the LVDEN bit. The LVDF bit located in the power status register (PMU_CS0) indicates whether V_{DD}/V_{DDA} is higher or lower than the LVD threshold voltage event. This event is connected to the 16th line of EXTI. The user can configure EXTI by Line 16 generates a corresponding interrupt. (LVD interrupt signal depends on the rising or falling edge configuration of EXTI line 16). The value of the hysteresis voltage V_{hyst} is 100mV.

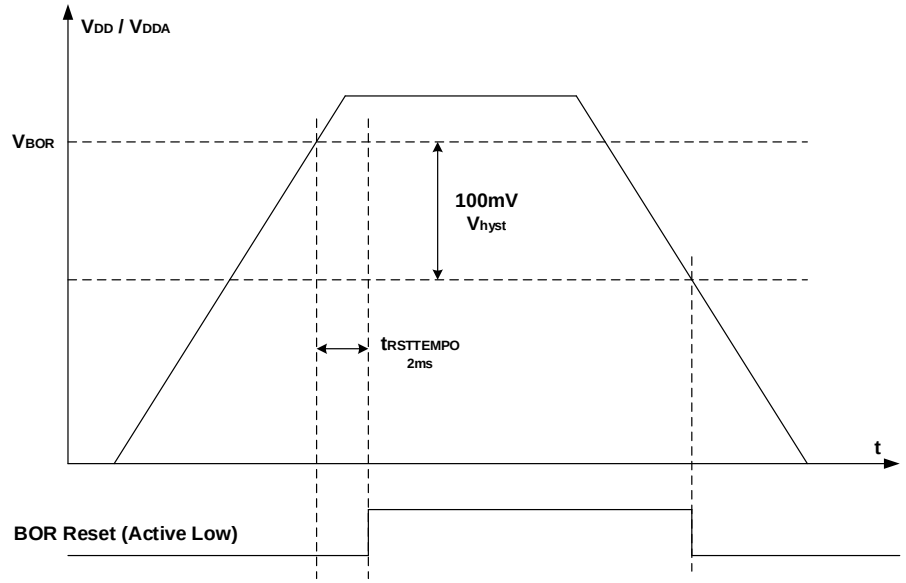
LVD application: When the MCU power supply is subject to external interference, such as a voltage drop, we can set the low voltage detection threshold (the threshold is greater than the PDR value) through LVD. Once it falls to the threshold, the LVD interrupt is turned on, which can be used in the interrupt function. Set operations such as soft reset to avoid other exceptions from the MCU.

Figure 2-4. LVD Threshold Waveform



The GD32E5xx series MCU also integrates a BOR circuit. The BOR circuit detects V_{DD}/V_{DDA} and generates a power reset signal to reset the entire chip except the backup domain when the voltage is lower than the threshold defined by BOR_TH of the option byte and the threshold is not 0b11 (default state: BOR_TH=0b11, BOR function is off). Regardless of whether the option byte BOR_TH has a value of 0b11, the POR/PDR (power-on/power-down reset) circuit will always be in the detection state. ***Figure 2-5. BOR Threshold Waveform*** shows the relationship between the supply voltage and the BOR reset signal. V_{BOR} represents the BOR reset threshold voltage, which is defined in the option byte BOR_TH. The value of the hysteresis voltage V_{hyst} is 100mV.

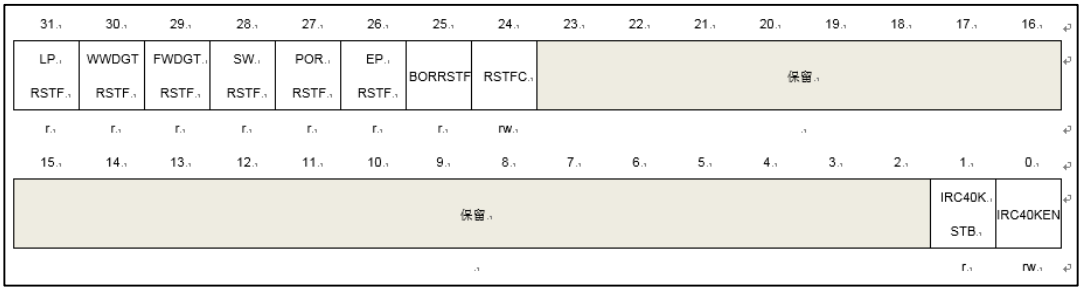
Figure 2-5. BOR Threshold Waveform



In addition, the MCU reset source can be judged by querying the register RCU_RSTSCK (0x40021024). This register can only clear the flag bit after a power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the

RSTFC control bit. When the watchdog is reset or other reset events, it can be more accurately reflected in the RCU_RSTSCK register.

Figure 2-6. RCU_RSTSCK Register



MCU integrates a power-up/power-down reset circuit. When designing an external reset circuit, a capacitor (typical value of 100nF) must be placed on the NRST pin to ensure that the power on the NRST pin generates a low pulse delay of at least 20us for completing effective power-on reset process.

Figure 2-7. System Reset Circuit

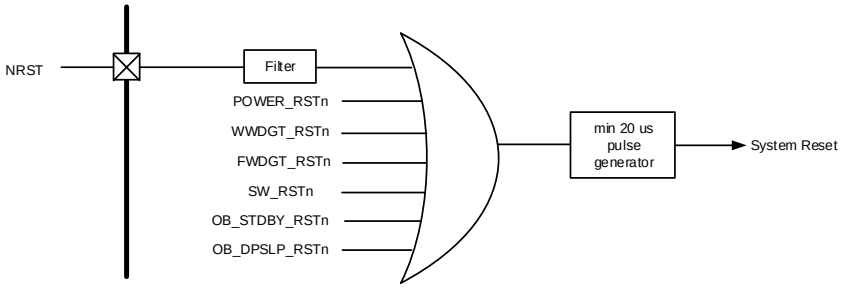
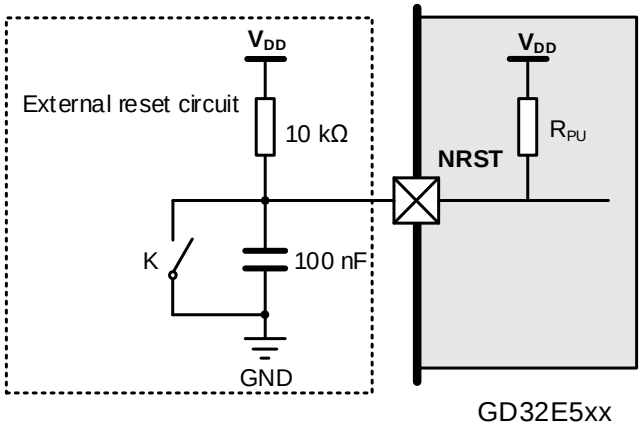


Figure 2-8. Recommend External Reset Circuit



Note:

1. The pull-up resistor is recommended to be 10kΩ, so that voltage interference will not cause the chip to work abnormally;
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin;
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit;
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of

NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

2.2. Clock

GD32E5xx series has a complete clock system inside, and you can choose a suitable clock source according to different applications. The main features of the clock:

- 4-32 MHz external high-speed crystal oscillator (HXTAL)
- Internal 8 MHz RC oscillator (IRC8M)
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- Internal 48 MHz RC oscillator (IRC48M)
- Internal 40 kHz RC oscillator (IRC40K)
- PLL clock source can be selected from HXTAL、IRC8M or IRC48M
- HXTAL clock monitor

GD32E503xx microcontrollers where the flash memory density ranges between 256 and 512 Kbytes are called High-density devices (GD32E5xx_HD).

GD32E505xx、GD32E507xx、GD32E508xx microcontrollers are called connectivity line devices (GD32E5xx_CL).

Figure 2-9. GD32E503xx Clock Tree

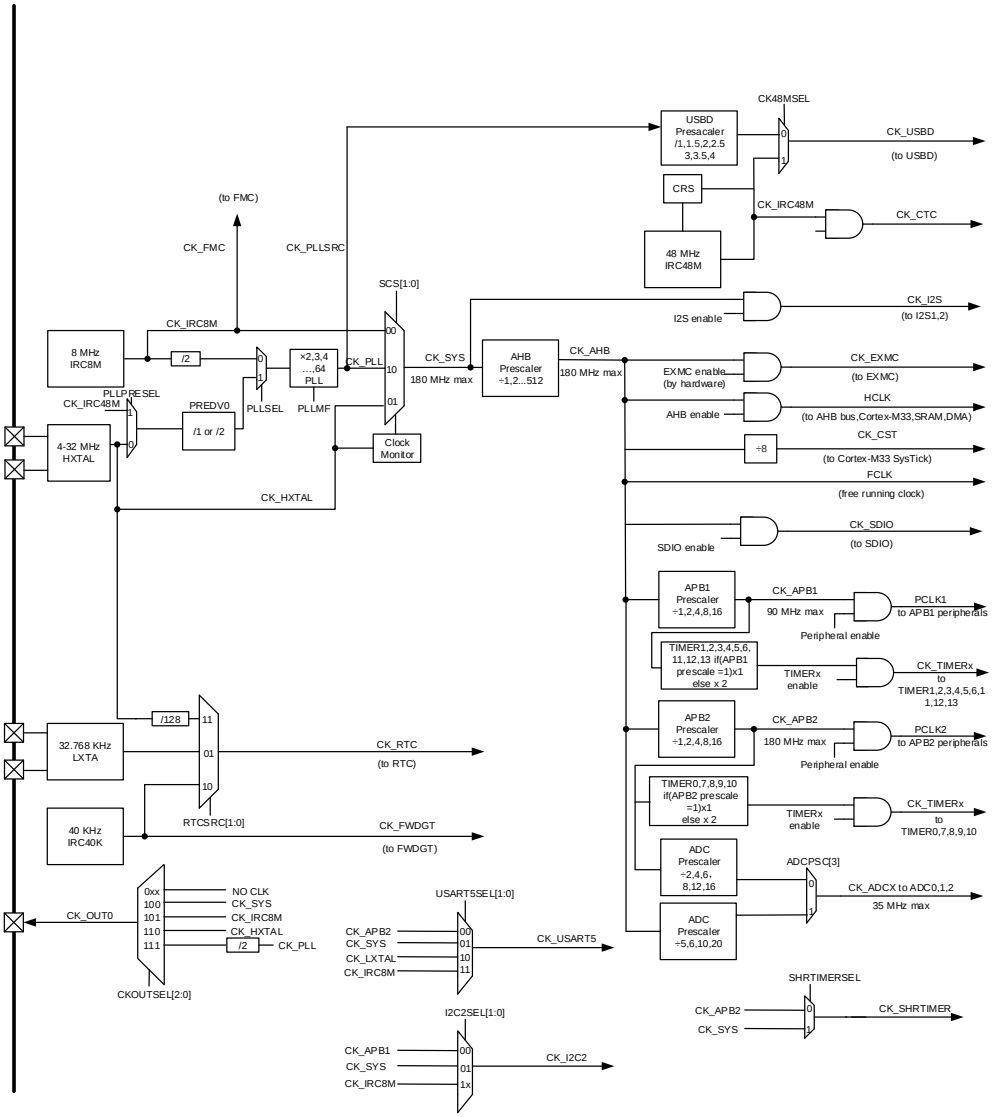
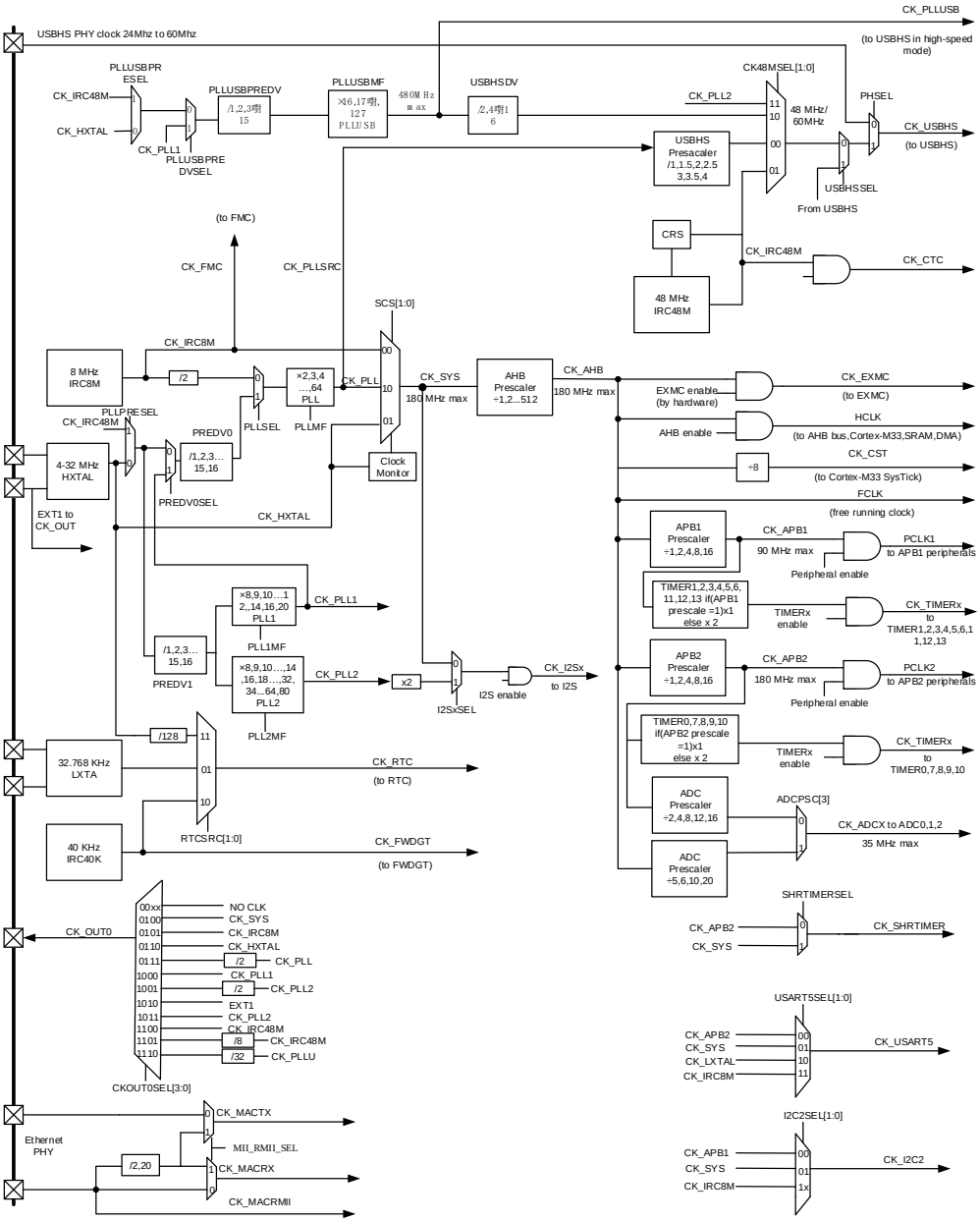


Figure 2-10. GD32E505xx / GD32E507xx / GD32E508xx Clock Tree



2.2.1. External high-speed crystal oscillator clock (HXTAL)

4-32MHz external high-speed crystal oscillator (passive crystal) can provide accurate main clock for the system. The crystal for that specific frequency must be placed close to the HXTAL pin, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the chosen oscillator parameters. HXTAL can also use the bypass input mode to input the clock source (1-50MHz active crystal oscillator, etc.). When the bypass input is used, the signal is connected to OSC_IN, and OSC_OUT remains floating. The Bypass function of HXTAL needs to be turned on in software (enable the HXTALBPS bit in RCU_CTL).

Figure 2-11. HXTAL External Crystal Circuit

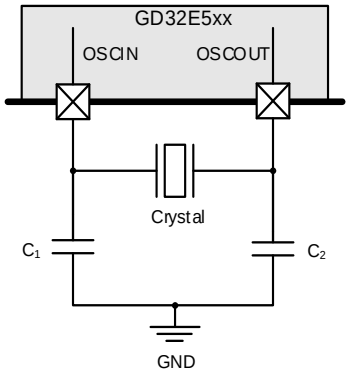
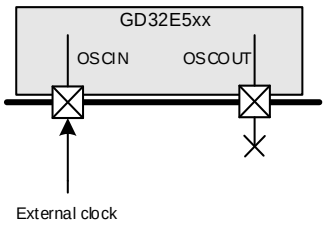


Figure 2-12. HXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC_IN, and OSC_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close to the crystal pin as possible.
3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU, causing the crystal to work abnormally, the external matching capacitor can be appropriately reduced.
4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.
5. Accuracy: external active crystal oscillator > external passive crystal > internal IRC16M.
6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}. If Bypass is not turned on, the amplitude requirements of the active crystal oscillator will be greatly reduced.
7. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSC_OUT and OSC_IN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator

cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.2.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768KHz low-speed external crystal (passive crystal), which can provide a low-power and high-precision clock source for RTC. The RTC module of the MCU is equivalent to a counter. The accuracy will be affected by the crystal performance, matching capacitance and PCB material. If you want to obtain better accuracy, it is recommended to connect PC13 to the timer input capture pin during circuit design. TIMER to calibrate LXTAL, and set the frequency division register of RTC according to the calibration situation. LXTAL can also support bypass clock input (active crystal oscillator, etc.), which can be enabled by configuring the LXTALBPS bit in RCU_BDCTL.

Figure 2-13. LXTAL External Crystal Circuit

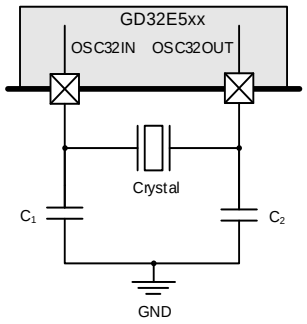
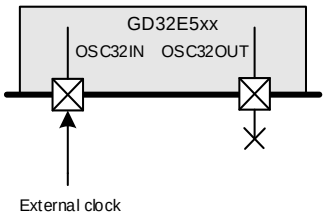


Figure 2-14. LXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC32_IN, and OSC32_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF-7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.
3. When the RTC selects IRC40K as the clock source and uses V_{BAT} for external independent power supply, if the MCU is powered off at this time, the RTC will stop

counting. After re-powering, the RTC will continue to count up with the previous count value. If the application needs to use V_{BAT} to power the RTC, the RTC can still time normally, and the RTC must select LXTAL as the clock source.

2.2.3. Clock Output Capability (CKOUT)

For GD32E503xx series MCU, you can select different clock signal output by configuring the CKOUT0SEL[2:0] bits of the clock register RCU_CFG0, and the corresponding GPIO pin PA8 needs to be configured as a multiplexing function to output the selected signal, as shown in the following:

Table 2-1. CKOUT0SEL[2:0] Control Bits

CKOUT0SEL[2:0]	Clock Source
0xx	NA
100	CK_SYS
101	CK_IRC8M
110	CK_HXTAL
111	CK_PLL/2

For GD32E505xx / GD32E507xx / GD32E508xx series MCU, you can select different clock signal output by configuring the CKOUT0SEL[3:0] bits of the clock register RCU_CFG0, and the corresponding GPIO pin PA8 needs to be configured as a multiplexing function to output the selected signal, as shown in the following:

Table 2-2. CKOUT0SEL[3:0] Control Bits

CKOUT0SEL[3:0]	Clock Source
00xx	NO CLK
0100	CK_SYS
0101	CK_IRC8M
0110	CK_HXTAL
0111	CK_PLL/2
1000	CK_PLL1
1001	CK_PLL2/2
1010	EXT1
1011	CK_PLL2
1100	CK_IRC48M
1101	CK_IRC48M/8
1110	CK_PLLUSB/32

2.2.4. HXTAL Clock Monitor (CKM)

Set the HXTAL clock monitoring enable bit CKMEN in the control register RCU_CTL, HXTAL can enable the clock monitoring function. This function must be enabled after the HXTAL start-up delay has elapsed and disabled after the HXTAL has been stopped. Once the HXTAL fault is detected, the HXTAL will be automatically disabled, and the HXTAL clock blocking interrupt

flag bit CKMIF in the interrupt register RCU_INT will be set to '1' to generate an HXTAL fault event. The interrupt caused by this fault is connected to the non-maskable interrupt NMI of the Cortex-M33.

Note: If HXTAL is selected as the system or PLL clock source, HXTAL failure will cause the IRC8M to be selected as the system clock source and the PLL will be automatically disabled. The clock source of the RTC needs to be reconfigured.

2.2.5. PLL Spread Spectrum (SSCG)

In order to reduce EMI interference, the GD32E5xx PLL integrates the clock spread spectrum function (only applicable to the main PLL), which effectively reduces the energy of the main clock frequency and its odd harmonics. According to the set modulation frequency f_{mod} and modulation peak mdamp (Refer to***Table 2-3. PLL spread spectrum clock generation (SSCG) characteristics***).

Calculate MODCNT and MODSTEP by formula 2-1 and formula 2-2, and fill in the PLL clock spread spectrum control register (RCU_PLLSSCTL). Note that the product of MODCNT and MODSTEP cannot be greater than 2^15-1. If it is greater than that, it is necessary to reduce the modulation peak mdamp and recalculate it.

Table 2-3. PLL spread spectrum clock generation (SSCG) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{mod}	Modulation frequency	—	—	—	10	kHz
mdamp	Peak modulation amplitude	—	—	—	2	%
MODCNT* MODSTEP	—	—	—	—	2^{15}-1	—

MODCNT and MODSTEP are obtained by the following formula:

$$MODCNT=round(f_{PLLIN}/4/f_{mod}) \quad (2\text{-}1)$$

$$MODSTEP = round(mdamp*PLLN*2^{14}/(MODCNT*100)) \quad (2\text{-}2)$$

f_{PLLIN} is the PLL input clock frequency, f_{mod} is the spread spectrum modulation frequency, mdamp is the spread spectrum modulation amplitude (expressed as a percentage), and PLLN is the PLL clock frequency multiplication factor.

For example, PLL reference clock source HXTAL = 8MHz, prescaler PLLM = 4, then f_{PLLIN} = 2MHz, set PLLN = 200 (at this time, the VCO frequency is 400MHz, and the system clock is 200MHz by dividing by two), the spread spectrum modulation frequency is 10KHz, and the modulation amplitude is 2 %, then MODCNT = 50 and MODSTEP = 1311 are calculated. At this time, MODCNT * MODCNT > 2^15 - 1, which cannot be achieved. Reduce the modulation amplitude to 1%, then MODCNT = 50, MODSTEP = 655, at this time MODCNT * MODCNT = 32750 < 2^15 - 1 meets the requirements.

According to the setting of SS_TYPE in the register RCU_PLLSSCTL, two types of spread spectrum modulation can be selected, namely center spread spectrum and downward spread spectrum, and the PLL output frequency will change as the following waveform.

Figure 2-15. Center Spread Spectrum

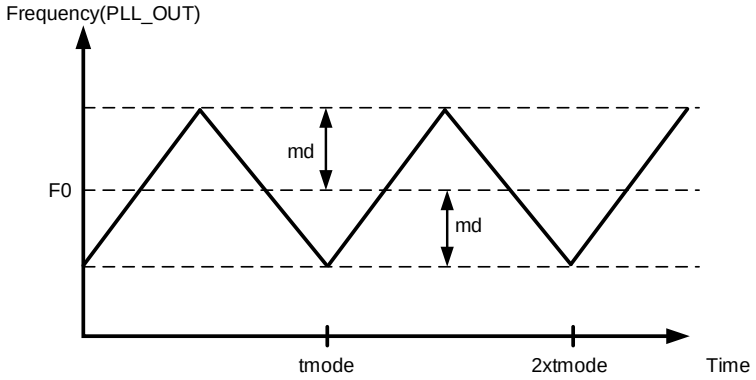
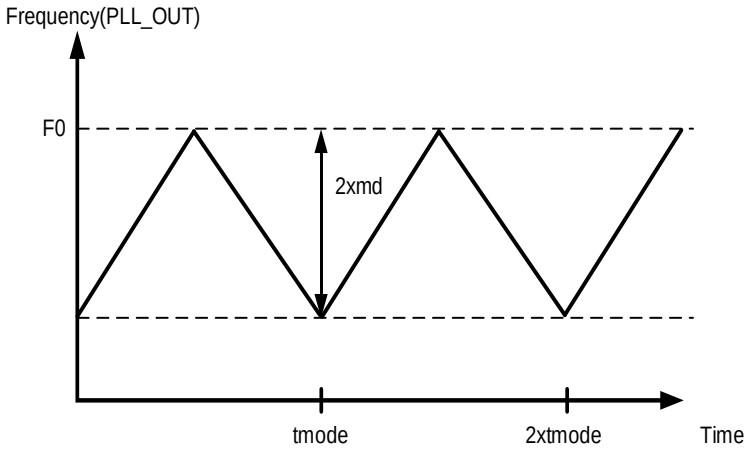


Figure 2-16. Down Spread Spectrum



2.2.6. Voltage control

The core voltage can be changed by configuring the DSPLPVS[2:0] bits of the clock register RCU_DSV.

Table 2-4. The core voltage in Deep-sleep mode

DSLPVS[2:0]	Deep-sleep mode voltage (V)
000	1.0
001	0.9
010	0.8
011	0.7

2.3. Startup Configuration

The GD32E5xx series provides three boot modes, which can be selected by the BOOT0 bit and the BOOT1 pin to determine the boot option.*Table 2-6. BOOT mode* are three startup configuration mode. When designing the circuit, run the user program, the BOOT0 pin cannot be left floating, it is recommended to connect a 10kΩ resistor to GND.*Figure 2-17.*

Recommend BOOT Circuit Design is recommended circuit design; when running the System Memory to update the program, you need to connect the BOOT0 pin to high and the BOOT1 pin to low. After the update is completed, the user program can be run after the BOOT0 is connected to a low level; the SRAM execution program is mostly used in the debugging status.

The embedded Bootloader is stored in the system storage space for reprogramming the FLASH memory. In the GD32E5xx device, Bootloader can interact with the outside world through USART0, USART1 or USB. The details are shown in *Table 2-5. Bootloader Interactive Interface*.

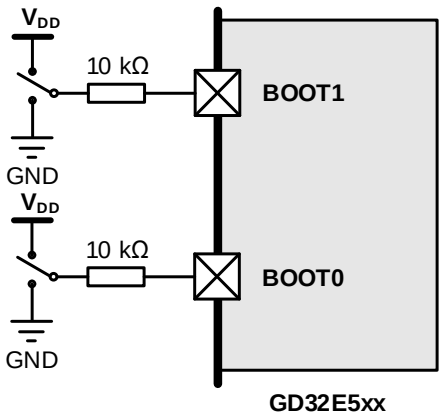
Table 2-5. Bootloader Interactive Interface

Product	MCU Part Numbers	Bootloader Interactive Interface
HD	GD32E503xx	USART0(PA9 PA10)
CL	GD32E505xx	USART0(PA9 PA10) USART1(PD5 PD6) USB(PA9 PA11 PA12)
	GD32E507xx	USART0(PA9 PA10) USART1(PD5 PD6) USB(PA9 PA11 PA12)
	GD32E508xx	USART0(PA9 PA10) USART1(PD5 PD6) USB(PA9 PA11 PA12)

Table 2-6. BOOT mode

BOOT mode	BOOT1	BOOT0
Main Flash Memory	X	0
System Memory	0	1
On Chip SRAM	1	1

Figure 2-17. Recommend BOOT Circuit Design



Note:

1. After the MCU is running, if the BOOT state is changed, it will take effect after the system

is reset. MCU.

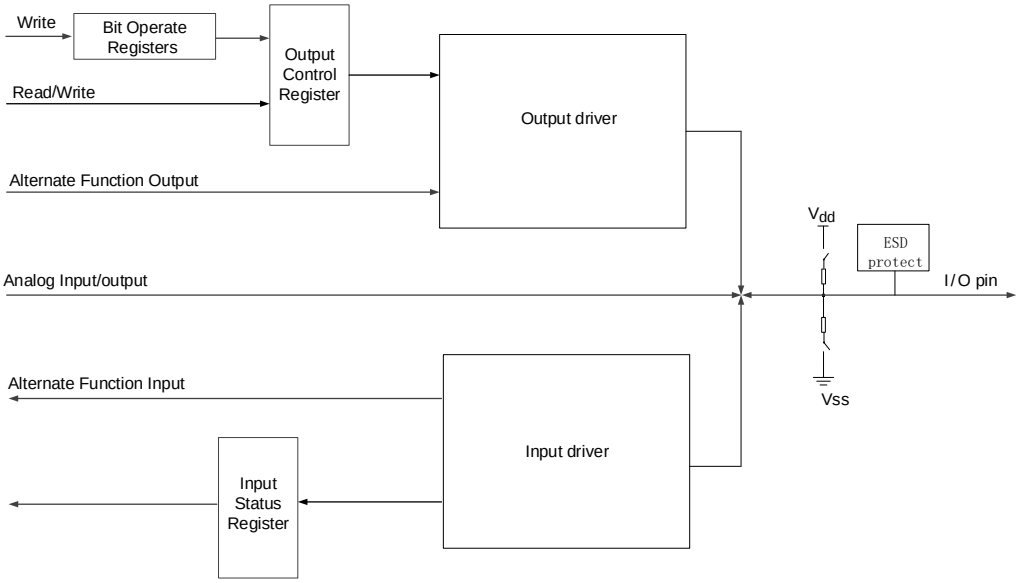
2. Once the BOOT1 pin state is sampled, it can be released for other purposes.

2.4. Typical Peripheral Modules

2.4.1. GPIO Circuit

The largest package GPIO interface includes 7 groups of general-purpose input/output ports, each group of ports provides up to 16 general-purpose input/output pins, which are PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15 and PG0 ~ PG15, each pin can be independently configured through registers, the basic structure of GPIO port is shown in ***Figure 2-18. Basic structure of standard IO***.

Figure 2-18. Basic structure of standard IO



Note:

1. The IO port is divided into 5V tolerant and non-5V tolerant. When using, pay attention to distinguish the IO port withstand voltage. For the GD32E5xx chip, except PA4 and PA5, the two pins are non-5V tolerant pins, and the other pins are 5V tolerant.
2. When the 5V-tolerant IO port is directly connected to 5V, it is recommended that the IO port be configured in open-drain mode and externally pull up to work.
3. After the IO port is powered on and reset, the default mode is floating input, and the level characteristics are uncertain. In order to obtain more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the corresponding mode according to application requirements (chip Ports that are not exported internally also need to be configured).
4. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.
5. The four IO ports of PC13, PC14, PC15 have weak drive capability and limited output current capability(about 3mA). When configured in output mode, their working speed

cannot exceed 2MHz.

6. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.

2.4.2. USART Circuit

Universal Synchronous Asynchronous Receiver Transmitter (USART) provides a flexible and convenient serial data exchange interface, and data frames can be transmitted in full-duplex or half-duplex, synchronous or asynchronous mode. The USART provides a programmable baud rate generator that divides the system clock to generate the specific frequency required for USART transmission and reception.

USART not only supports the standard asynchronous transceiver mode, but also implements some other types of serial data exchange modes, such as infrared coding specification, SIR, smart card protocol, LIN, and synchronous single-duplex mode. It also supports multiprocessor communication and Modem flow control operation (CTS/RTS). Data frames support transmission from the LSB or MSB. Both the polarity of the data bits and the TX/RX pins can be flexibly configured.

USART supports DMA function to realize high-speed data communication.

Table 2-7. USART Important Pin Description

Pin	Type	Description
RX	Input	Receive data
TX	Output I/O (Single-Wire Mode/Smart Card Mode)	Send data, when USART is enabled, if no data is sent, the default is high level.
CK	Output	Serial clock signal for synchronous communication
nCTS	Input	Hardware flow control mode send enable signal
nRTS	Output	Hardware flow control mode send request signal

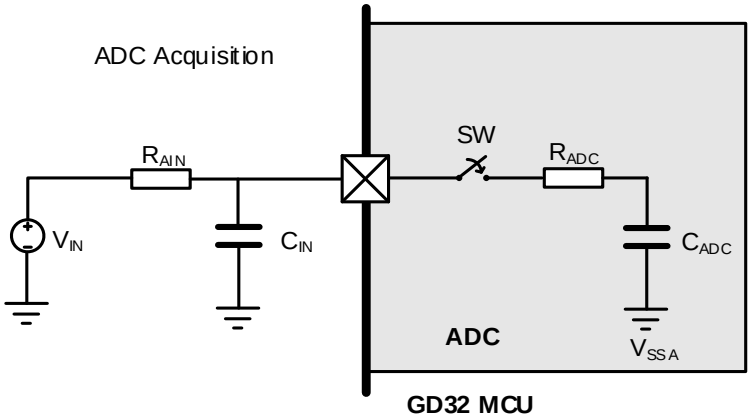
2.4.3. ADC Circuit

The GD32E5xx series integrates a 12-bit SAR ADC, which has up to 18 channels and can measure 16 external and 2 internal signal sources. The internal signal is the temperature sensor channel (ADC0_CH16) and the internal reference voltage input channel (ADC0_CH17). The temperature sensor reflects the change in temperature and is not suitable for measuring absolute temperature. If accurate temperature measurement is required, an external temperature sensor must be used. The internal reference voltage V_{REFINT} provides a regulated voltage output (1.1V) to the ADC and is internally connected to ADC0_IN17.

If the ADC collects the external input voltage during use, if the sampled data fluctuates greatly, it may be due to the interference caused by power supply fluctuations. You can calibrate by sampling the internal V_{REFINT} and then calculate the externally sampled voltage.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin. It is recommended to place a small capacitor of 500pF. ADC supply requirements: the typical power supply voltage is 3.3V. When supply voltage is 1.62V to 2.4V, ADC maximum frequency is 14MHz, When supply voltage is 2.4V to 3.6V, ADC maximum frequency is 35MHz.

Figure 2-19. ADC Acquisition Circuit Design



When f_{ADC} = 35MHz, the relationship between the input impedance and the sampling period is as follows. In order to obtain better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible during use, and select a larger value for the sampling period. When designing external circuits, try to reduce the input Impedance, if necessary, use the op amp to follow to reduce the input impedance.

Table 2-8. f_{ADC} = 35MHz Relationship between sampling period and external input impedance

T_s (cycles)	t_s (μs)	$R_{AIN\ max}$ (kΩ)
1.5	0.043	0.6
7.5	0.21	5.0
13.5	0.39	9.4
28.5	0.81	20.5
41.5	1.19	30.0
55.5	1.59	40.0
71.5	2.04	52.0
239.5	6.84	175.8

2.4.4. DAC Circuit

The digital/analog converter of GD32E5xx series MCU can convert 12-bit digital data to voltage output on external pins. Data can be in 8-bit or 12-bit mode, left-justified or right-justified. When external triggering is enabled, DMA can be used to update digital data on the input. At the output voltage, higher drive capability can be obtained by enabling the DAC output buffer. The two DACs can work independently or concurrently.

Table 2-9. DAC Related Pin Description

Name	Description	Signal type
V_{DDA}	Analog power	Input, Analog power
V_{SSA}	Analog power ground	Input, Analog power ground
V_{REFP}	DAC positive reference voltage, $2.4V \le V_{REFP} \le V_{DDA}$	Input, Analog positive reference voltage
DAC_OUTx	DACx analog output	Analog output signal

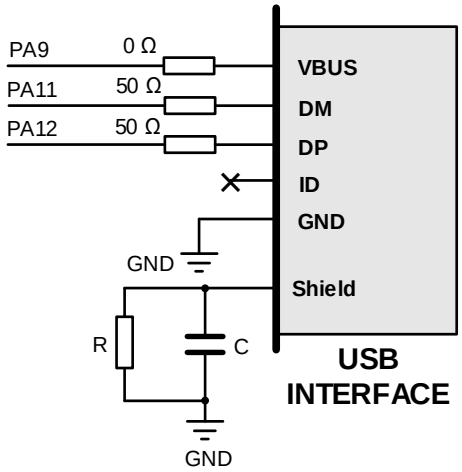
Before enabling the DAC module, the GPIO port (PA4 corresponds to DAC0, PA5 corresponds to DAC1) should be configured in analog mode.

2.4.5. USB Circuit

GD32E505xx / GD32E507xx / GD32E508xx interconnected MCU has a built-in USB interface, which is a USBFS module. The USB protocol requires a clock accuracy of not less than 500ppm, and the internal clock may not be able to achieve such accuracy, so it is recommended to use an external crystal or an active crystal oscillator as the USB module clock source when using the USB function.

GD32E503x can only be designed as a USB device. When designing the circuit, a controllable 1.5K pull-up resistor needs to be designed for the DP data line. The recommended USB-Device reference circuit is shown in ***Figure 2-20. Recommend USB-Device Reference Circuit***. In order to improve the ESD performance of USB, it is recommended to design a resistance-capacitance discharge isolation circuit for the USB case.

Figure 2-20. Recommend USB-Device Reference Circuit

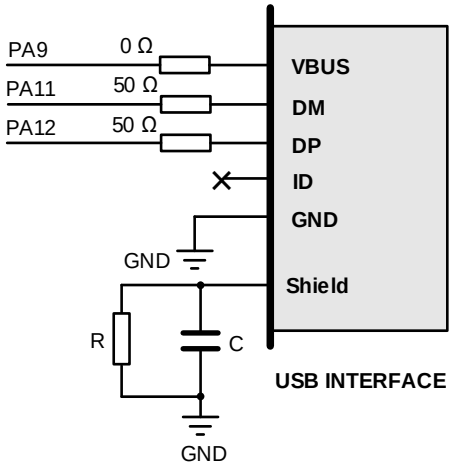


Recommendation: R = 1MΩ, C = 4700pF

The USB module of GD32F505xx / GD32F507xx interconnected MCU can be designed as both USB device and USB host. The recommended circuit when designed as Device is shown in ***Figure 2-21. Recommend USB-Device (USBFS) Reference Circuit***; when designed as Device, if PA9 is connected to VBUS, the DP line does not need an external 1.5K pull-up resistor; if PA9 is not connected To VBUS, if the VBUSIG control bit in the USBFS_GCCFG

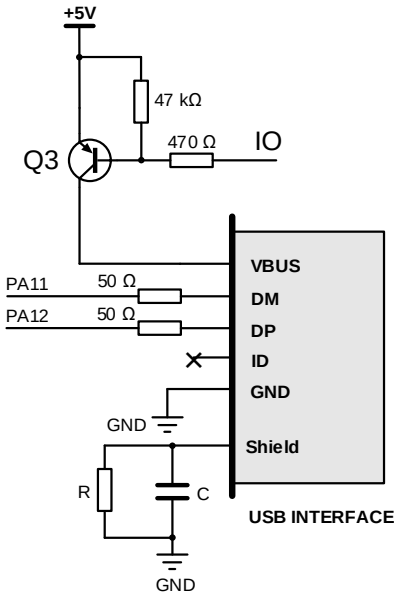
register has been configured, the USB_DP data line can not be connected with a 1.5K pull-up resistor. If this register is not configured, the USB_DP data line needs to be connected with a 1.5K pull-up resistor. In order to improve the ESD performance of USB, it is recommended to design a resistance-capacitance discharge isolation circuit for the USB case. When designing in host mode, the recommended circuit is shown in ***Figure 2-22. Recommend USB-Host Reference Circuit***

Figure 2-21. Recommend USB-Device (USBFS) Reference Circuit



Recommendation: R = 1MΩ, C = 4700pF

Figure 2-22. Recommend USB-Host Reference Circuit



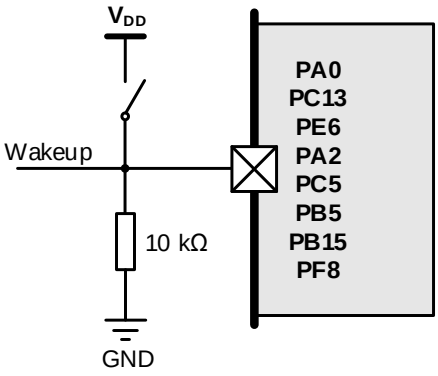
Recommendation: R = 1MΩ, C = 4700pF

2.4.6. Standby mode wake-up circuit

The GD32E5xx series series supports five low-power modes, namely sleep mode, deep-sleep mode、deep-sleep 1、deep-sleep 2 mode and standby mode. The standby mode with the

lowest power consumption is the standby mode, which requires the longest wake-up time. Wake-up from Standby mode can be woken up by the rising edge of the WKUP pin. At this time, there is no need to configure the corresponding GPIO, just configure the WUPEN bit in the PMU_CS register. The WKUP wake-up pin reference circuit is designed as follows::

Figure 2-23. Recommend Standby external wake-up pin circuit design



Note: In this mode, attention should be paid to the circuit design. If there is a series resistance between the WKUP pin and V_{DD}, additional power consumption may be added.

2.5. Download the debug circuit

GD32E5xx series cores support JTAG debug interface and SWD debug interface. The JTAG interface standard is a 20-pin interface, including 5 signal interfaces, and the SWD interface standard is a 5-pin interface, including 2 signal interfaces.

Note: After reset, the debug related ports are in input PU/PD mode, where:
PA15: JTDI is in pull-up mode.
PA14: JTCK/SWCLK in pull-down mode.
PA13: JTMS/SWDIO in pull-up mode.
PB4: NJTRST is in pull-up mode.
PB3: JTDO is floating mode.

Table 2-10. JTAG download debug interface assignment

Alternate function	GPIO port
JTMS	PA13
JTCK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

Figure 2-24. Recommend JTAG Wiring Reference Design

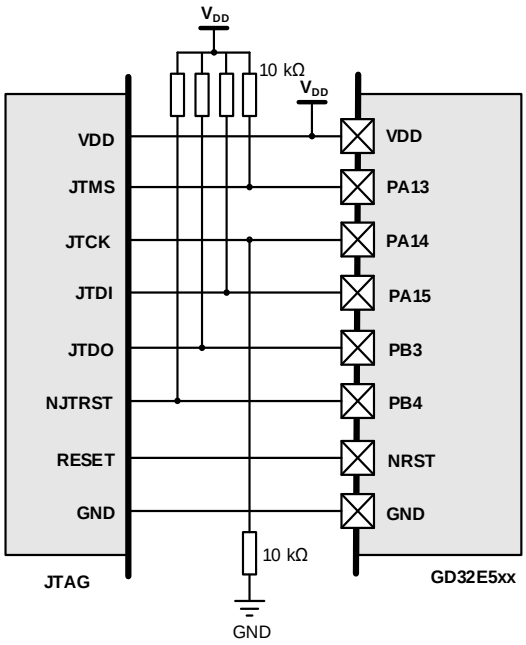
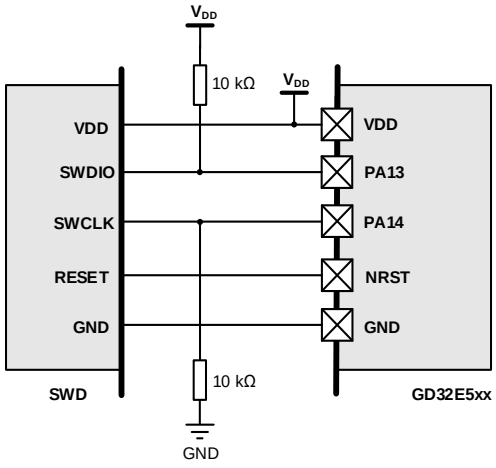


Table 2-11. SWD Download Debug Interface Assignment

Alternate function	GPIO port
SWDIO	PA13
SWCLK	PA14

Figure 2-25. Recommend SWD Wiring Reference Design

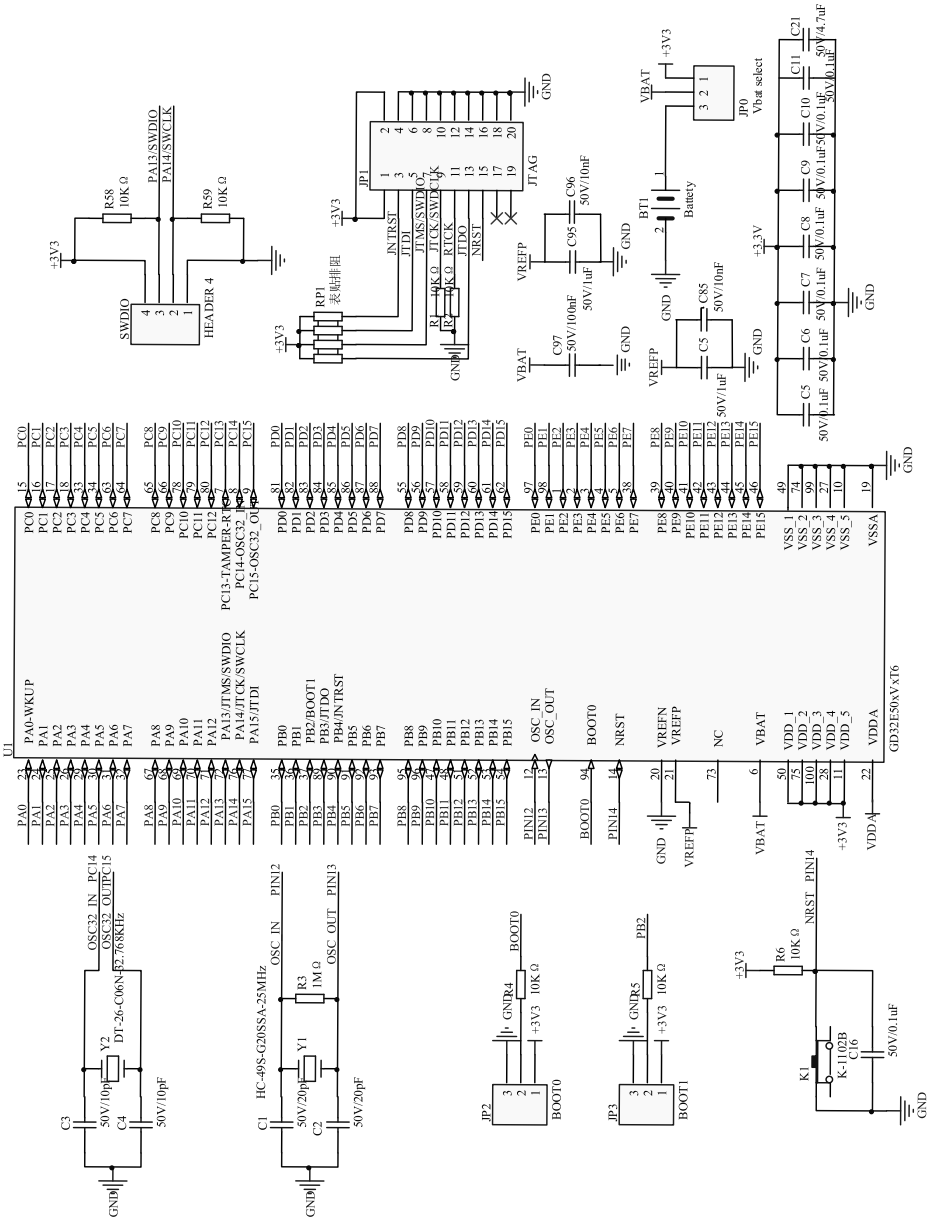


There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100Ω ~ 1kΩ resistor.

2.6. Reference Schematic Design

Figure 2-26. GD32E5xx Recommend Reference Schematic Design



3. PCB Layout Design

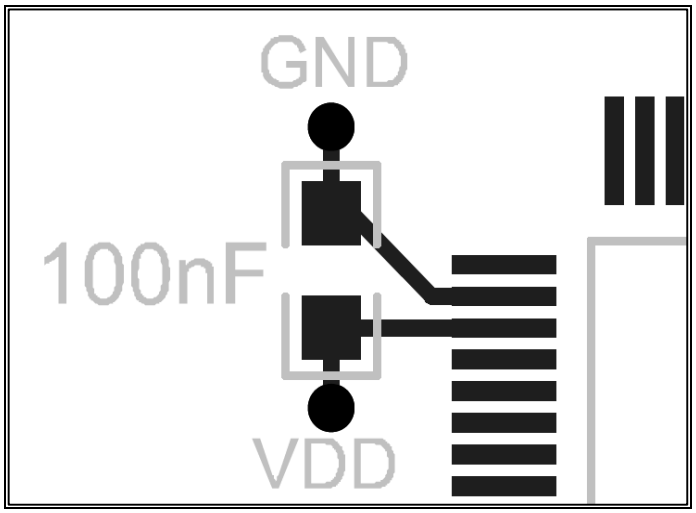
In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design solution with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

3.1. Power Supply Decoupling Capacitors

The GD32E5xx series power supply has three power supply pins: VDD, VDDA and VBAT. The 100nF decoupling capacitor can be made of ceramic, and it is necessary to ensure that the position is as close to the power supply pin as possible. The power trace should try to make it pass through the capacitor first and then reach the MCU power pin, It is recommended to punch holes near the capacitor pad to connect with GND.

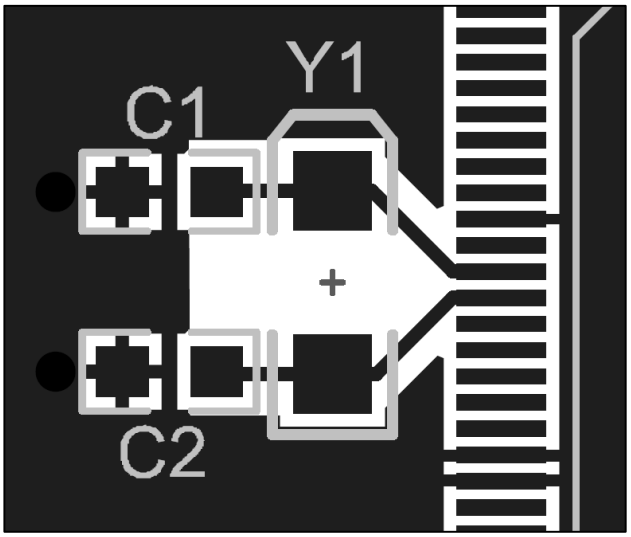
Figure 3-1. Recommend Power Pin Decoupling Layout Design



3.2. Clock Circuit

GD32E5xx series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)



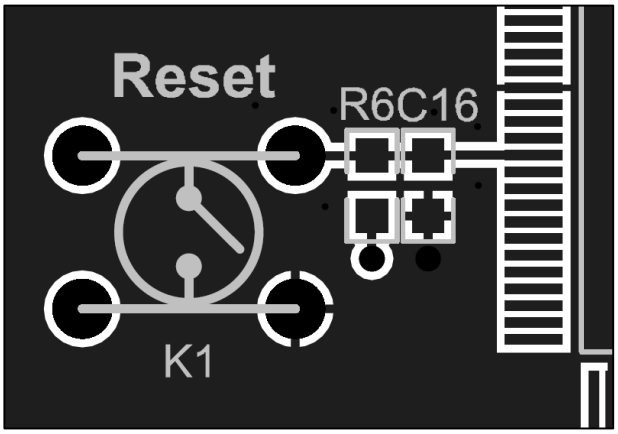
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.3. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-3. Recommend NRST Trace Layout Design



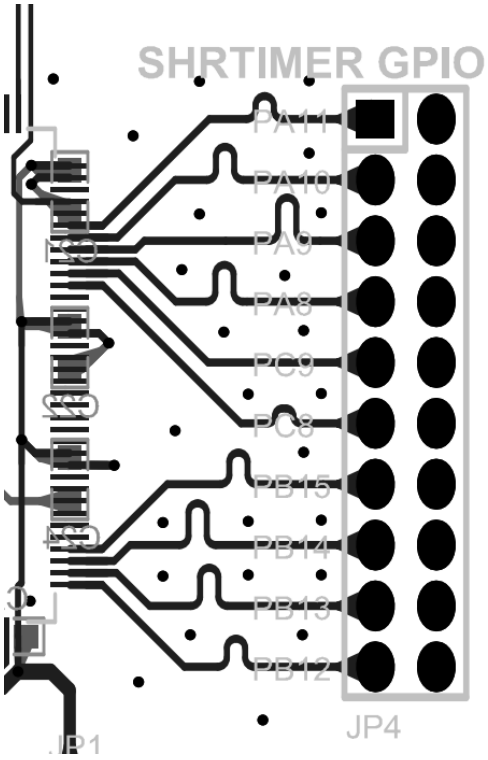
Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better

to wrap the NRST traces for better shielding effect.

3.4. SHRTIMER Circuit

SHRTIMER has a super high-resolution counting clock and can be used for high-precision timing. It can generate 10 super high resolution and flexible digital signals to control motor or be used for power management applications. The 10 digital signals can be output independently or coupled into 5 pairs of complementary signals.When used as multi-channel PWM output, it is recommended to use equal length and equal width lines for the output signal lines, eliminating interference from PCB traces to SHRTIMER resolution. The trace layout is shown in the figure:

Figure 3-4. Recommend SHRTIMER multi-channel PWM Trace Layout Design



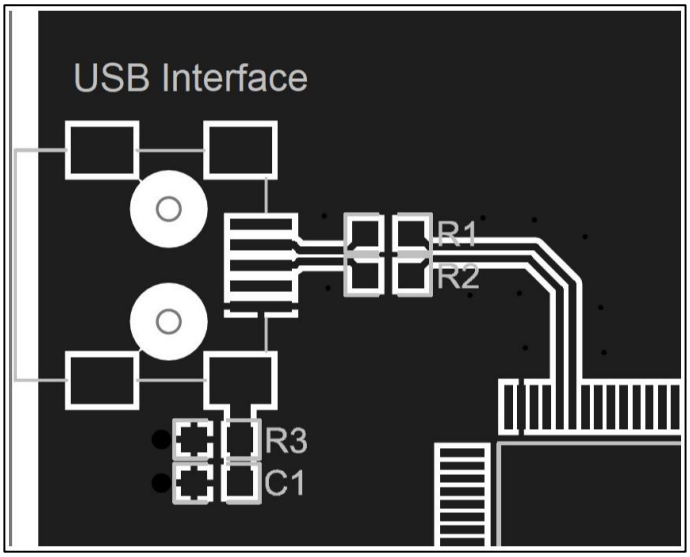
3.5. USB Circuit

The USB module has two differential signal lines, DM and DP. It is recommended that the PCB traces require a characteristic impedance of 90ohm. The differential traces should be run in strict accordance with the rule of equal length and equal distance, and the traces should be kept as short as possible. If the two differential lines are not equal in length , the short line can be compensated with a serpentine line at the terminal.

Due to impedance matching considerations, the series matching resistance is recommended to be about 50Ω. When the USB terminal interface is far away from the MCU, the series resistance value needs to be appropriately increased.

The USB differential trace reference is as follows:

Figure 3-5. Recommend USB Differential Trace Layout Design



Recommendation: R1 = R2 = 50Ω, R3 = 1MΩ, C = 4700pF

Note:

1. Reasonable placement during layout to shorten the differential trace distance.
2. Draw differential lines first, try not to exceed two pairs of vias for a pair of differential lines, and place them symmetrically.
3. Symmetrical parallel wiring to ensure that the two lines are tightly coupled, avoiding 90°, arc or 45° wiring.
4. Devices such as resistance-capacitor, EMC connected to the differential traces, or test points should also be symmetrical.

4. Package Description

GD32E5xx series has a total of 5 package types, namely LQFP48, LQFP64, LQFP100 and LQFP144.

Table 4-1. Package Description

Ordering code	Package
GD32E5xxCxT6	LQFP48(7x7, 0.5 pitch)
GD32E5xxRxT6	LQFP64(10x10, 0.5 pitch)
GD32E5xxVxT6	LQFP100(14x14, 0.5 pitch)
GD32E5xxZxT6	LQFP144(20x20, 0.5pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Dec.18, 2022
1.1	Update section 2.1.3 to provide all packaging power supply design drawings, explaining the connection of relevant pins within the chip	Jun. 21, 2023
1.2	Update GD32E50x to GD32E5xx. Add three series GD32E513/517/518xx to applicable products	Apr. 23, 2024

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