GigaDevice Semiconductor Inc.

GD32W515 Hardware Development Guide

Application Note
AN066

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1.   Introduction

This paper is designed for developers of 32-bit general purpose MCU GD32W515 series based on Arm®Cortex®-M33 architecture and Trustzone highly integrated 2.4GHz Wi-Fi system-on-chip(SOC). The hardware development of GD32W515 series products is generally introduced.Such as power supply, reset, clock, RF circuit and so on.The purpose of this application note is to enable developers to quickly use GD32W515 series products, develop and use product hardware quickly, save the time of reading manuals, and speed up the progress of product development.

This application note is divided into seven parts:

1.   Power supply, mainly introduces GD32W515 series power management, power supply design;
2.   Reset, mainly introduces the design of GD32W515 series reset function and mode selection;
3.   RF, mainly introduces the design of GD32W515 series RF circuit;
4.   Clock, mainly introduces the function design of GD32W515 series high and low speed clock;
5.   Refer to circuit and PCB Layout design, mainly introduce GD32W515 series hardware circuit design and PCB Layout design matters needing attention;
6.   Packaging description, mainly introduces the packaging forms and naming of GD32W515 series.

Table 1-1. Applicable Products

Type	Part Numbers
MCU	GD32W515xx series

2. Hardware design

The schematic diagram of GD32W515 series MCU module is shown in ***Figure 2-1. Circuit diagram of GD32W515 series MCU module***:

■ Power supply circuit design

■ Reset and mode selection circuit design

■ RF circuit design

■ XTAL circuit design

■ LXTAL circuit design

Figure 2-1. Circuit diagram of GD32W515 series MCU module
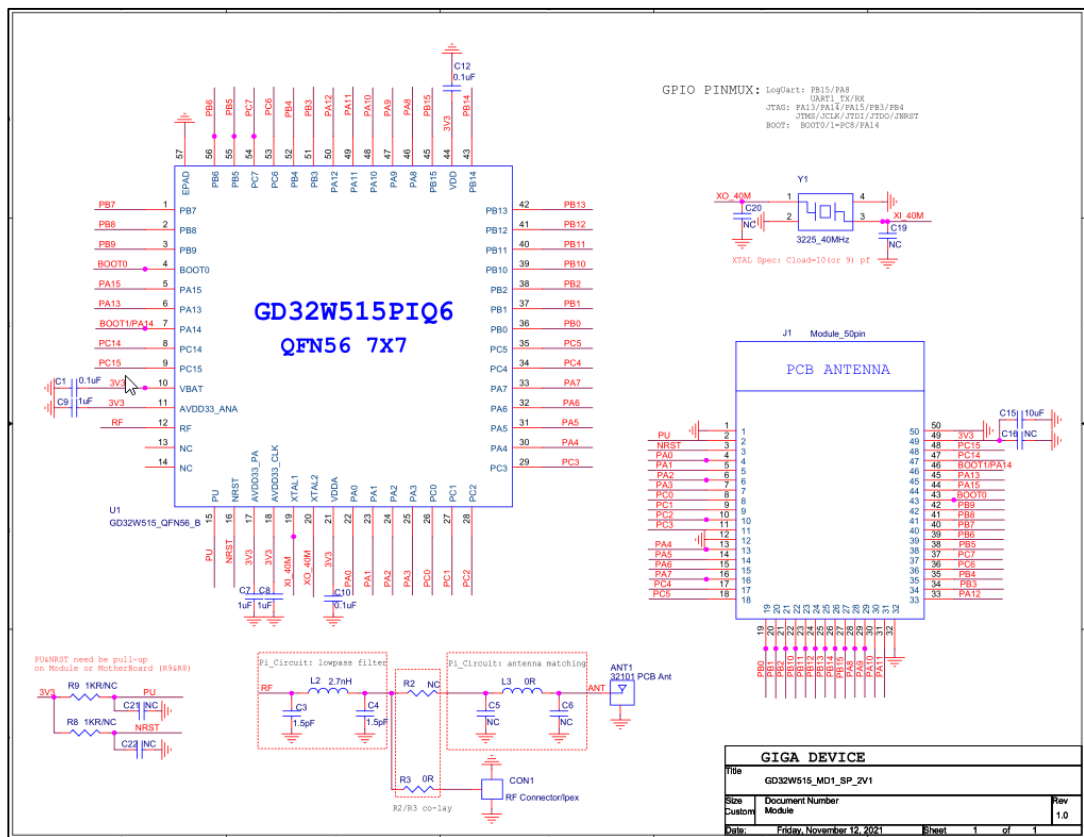
2.1. Power supply

GD32W515 series MCU module power pins can be divided into MCU RF part power pins and other parts of MCU (digital, analog, etc.) power pins. The former includes AVDD33_ANA(Pin11), AVDD33_PA(Pin17), AVDD33_CLK(Pin18). The latter includes VBAT(Pin10), VDDA (Pin21), VDD (Pin44), and the standard operating voltage of the above power pins is 3.3V.

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AVDD33_ANA(Pin11), AVDD33_PA(Pin17), AVDD33_CLK(Pin18). The latter includes VBAT(Pin10), VDDA (Pin21), VDD (Pin44), and the standard operating voltage of the above power pins is 3.3V.

It is recommended to place a large capacitor and a small capacitor at the module power entrance (as shown in **_Figure 2-2. Circuit at the module power_**). By default, only a large capacitor (such as 10uF) can be installed. At the same time, a separate filter capacitor is placed on each power pin. For RF power pins such as AVDD33_ANA, AVDD33_PA, AVDD33_CLK, 1uF filter capacitor is recommended (as shown in **_Figure 2-3. RF power pin circuit of the chip_**); For VBAT, VDDA, VDD and other power pins, 0.1uF filter capacitor can be selected (as shown in **_Figure 2-4. Circuit of other power pins of the chip_**).

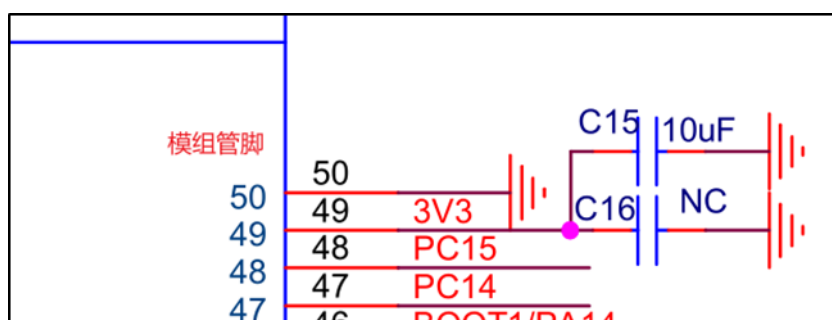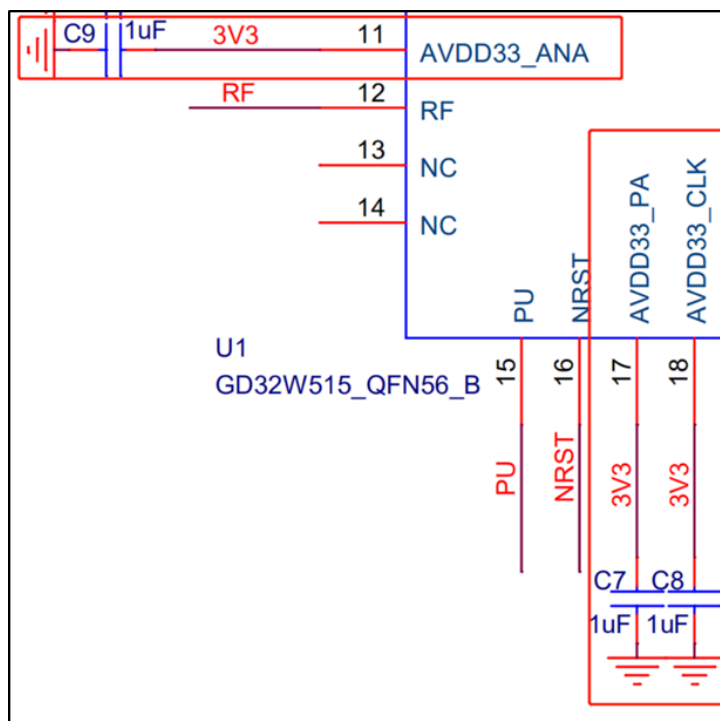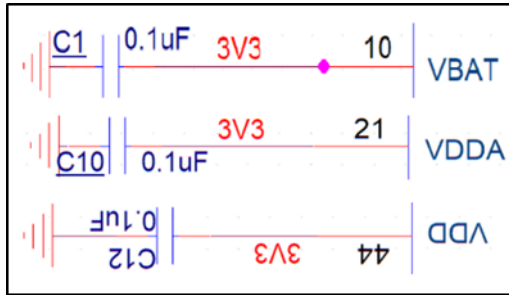**Figure 2-2. Circuit at the module power**

Figure 2-3. RF power pin circuit of the chip

When the W515 does not use the Wi-Fi function, AVDD33_CLK normally supplies power and attaches a 1uF decoupling capacitor. It is recommended that AVDD33_PA and AVDD33_ANA supply power without decoupling capacitor to save BOM.

Figure 2-4. Circuit of other power pins of the chip

2.2. Reset and mode selection circuit

GD32W515 pins PU(Pin15) and NRST(Pin16) are used to enable and reset the chip power respectively. The chip can only work when both pins are raised. The filter capacitor and pull-up resistor can be placed near the pin during the design. If there is a bottom plate, the pull-up resistor and filter capacitor can also be made on the bottom plate. In practice, only one of them needs to be selected as the enabling pin, while the other still needs to be connected to the pull resistor and filter capacitor. If GD32W515 is used as the master MCU, it is recommended to use NRST as the enabling pin, and the PU is always raised. If the GD32W515 is used as a slave device, you are advised to use PU as the enabling pin, and the NRST is always raised.

Boot mode selection pins of GD32W515 are BOOT0(Pin4) and BOOT1(Pin7). The definitions of these modes are shown in *Table 2-1. BOOT Mode*. It is usually recommended that its up/down resistors be placed on the base plate; For single module use, reserve up/down resistors at the module end. The reference design is shown in *Figure 2-5. Reset and mode selection circuit*, pull-down resistor is placed on the base plate.

Table 2-1. BOOT Mode

BOOT1	BOOT0	Boot Mode
X	0	Flash
0	1	Legacy Bootloader
1	1	SRAM

Figure 2-5. Reset and mode selection circuit
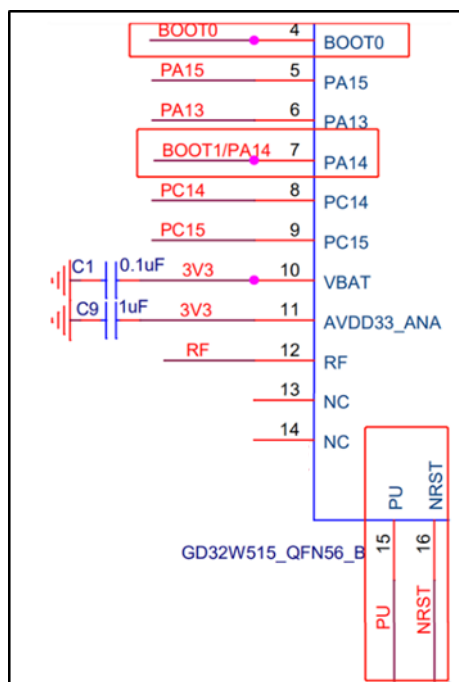
PU is pull-up. When the MCU is used as a slave device, the PU pin is raised to enable W515, and the PU pin is pulled down to disable W515.

2.3. RF circuit

The reference design of GD32W515 RF circuit is shown in ***Figure 2-6. RF circuit design***.The RF pin of the chip is Pin12, and there is a set of π-type (CLC combination) matching circuit on the path, which is mainly used to filter out the high-order harmonics of RF emission signals (to meet the certification requirements) and give consideration to impedance matching debugging; The capacitor and inductor in the matching circuit must be RF specifications materials, and the accuracy must be ±0.1pF(nH). The default matching circuit component combination is 1.5pF + 2.7nH + 1.5pF. The final use value shall be subject to the actual debugging results of different PCB. If no matching device is added, 0R resistance is recommended for series components by default, and NC resistance is recommended for parallel components. The antenna can use PCB antenna or external antenna, it is recommended to reserve RF test seat to facilitate conduction test and external antenna test; At the same time, reserve a π-type network for antenna matching.

Figure 2-6. RF circuit design
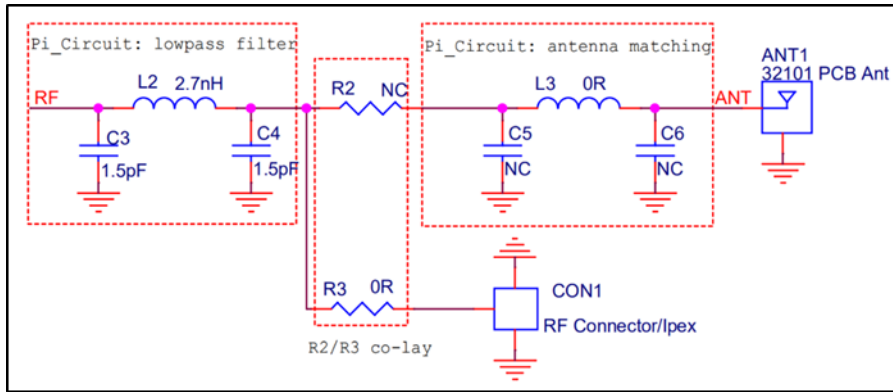
2.4.   XTAL circuit

GD32W515 module supports 40M, 26M and other frequency patch passive crystal, the default frequency is 40MHz, and the package can choose 3225, 2520, etc. The crystal circuit of GD32W515 series MCU refer to *Figure 2-7. Crystal circuit*. The two load capacitors are not attached (NC) by default. The frequency offset can be corrected by adjusting the internal capacitance of the chip. Consider the load capacitance NC, the load capacitance of the crystal must be 10pF (or 9pF) specifications (The Load Capacitance index in *Figure 2-8. Recommended crystal index*) . For other specifications, see the content in the red box.
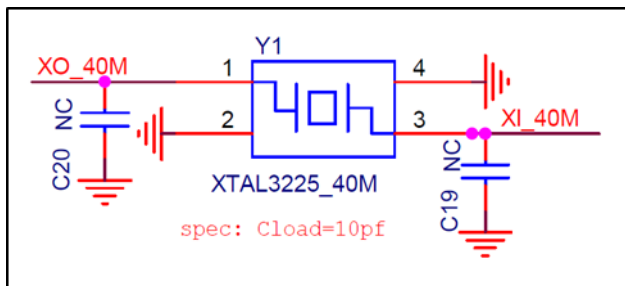
Figure 2-7. Crystal circuit

Figure 2-8. Recommended crystal index

	Parameters	SYM.	Electrical Spec.				Notes
			MIN	TYPE	MAX	UNITS	
1	Nominal Frequency	FL		40.000000		MHz	-
2	Oscillation Mode	-		Fundamental		-	-
3	Load Capacitance	CL		10		pF	-
4	Frequency Tolerance	-		±10		ppm	at 25 ℃ ± 3 ℃
5	Frequency Stability	-		±10		ppm	Over Operating Temp. Range (Reference 25℃)
6	Operating Temperature	-	-30	~	85	℃	-
7	Aging	-		±3		ppm	1st Year
8	Drive Level	DL	-	100	500	µW	-
9	Effective Resistance Rr	Rr	-	-	30	Ω	-
10	Shunt Capacitance C0	C0	-	-	3	pF	-
11	DLD2	-	-	-	10	Ohms	-
12	FDLD	-	-	-	10	ppm	-
13	SPDB	-	-	-	-3	dB	-
14	Insulation Resistance	-	500	-	-	MΩ	at DC 100V
15	Storage Temperature Range	-	-40	~	85	℃	-

2.5. LXTAL circuit

LXTAL crystal is a 32.768kHz low speed external crystal (passive crystal), which can provide a low power and high precision clock source for RTC.

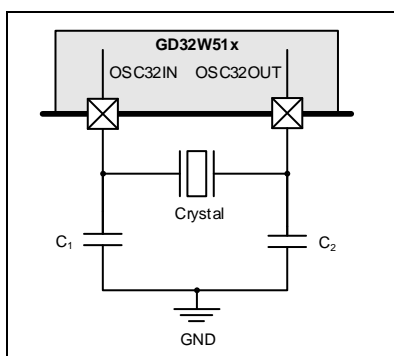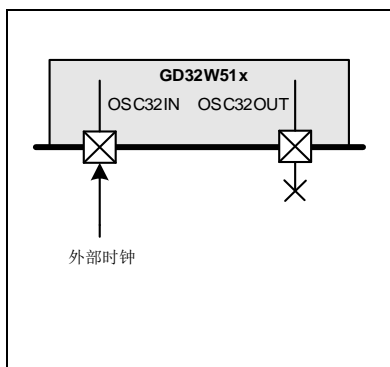**Figure 2-9. LXTAL external crystal circuit**

**Figure 2-10. LXTAL external clock circuit**

Note：

1.   In bypass mode, the signal is input from OSC32_IN and the OSC32_OUT is suspended;

2.   For the value of external matching capacitance, please refer to the formula $C_1 = C_2 = 2*(C_{LOAD}-C_S)$, where C_S is the stray capacitance of PCB and MCU pins, and the empirical value is between 2pF and 7pF, so 5pF is recommended as the reference value for calculation. When selecting an external crystal, it is recommended that the load capacitance of the crystal should be around 10pF, so that the capacitor values of C_1 and C_2 connected to the external matching capacitor should be 10pF, and the PCB layout should be as close as possible to the crystal pin;

3.   When the RTC selects IRC32K as the clock source and uses VBAT external independent power supply, if the MCU is powered off at this time, the RTC will stop counting, and after the restart, the RTC will continue to accumulate the previous counting value.   If the application needs to use VBAT to supply power to the RTC, the RTC can still time properly, and the RTC must select LXTAL as the clock source;

4.   MCU can set the driving capacity of LXTAL. If it is difficult to vibrate the external low-speed crystal during actual debugging, the driving capacity of LXTAL can be adjusted to high driving capacity.

3. PCB Layout Design

The Layout of GD32W515 module reference design is shown in ***Figure 3-1. GD32W515 module layout***.

Figure 3-1. GD32W515 module layout
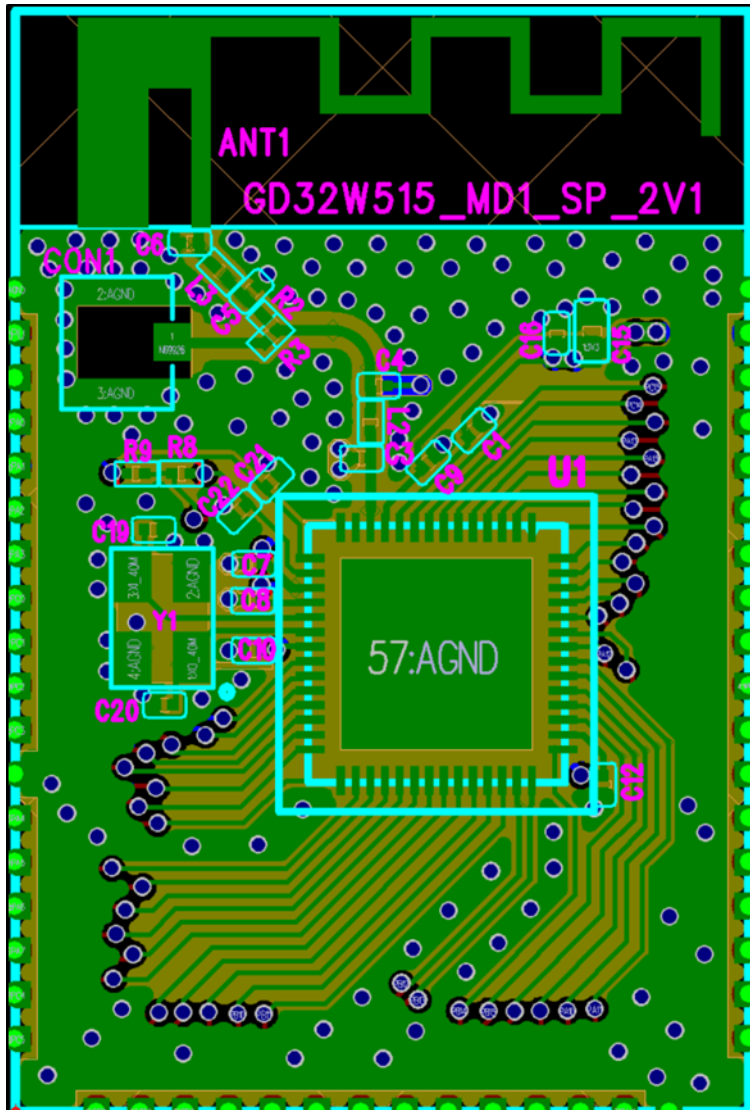
In the Layout design of GD32W515 module, the following parts should be noted:

- PCB stack design;
- Power supply network;
- RF circuit design;
- XTAL circuit design;
- GND Integrity & EPAD design;
- Shield design;
- Routing & Ploygon design.

3.1. PCB Stack Design

GD32W515 module PCB stacking should be designed with four layers, and the layer definition can be referred to *__Table 3-1. Refer to the PCB layer definition__*：

Table 3-1. Refer to the PCB layer definition

| The layer number of board	Four layer board
Reference layer Definition	Layer1：SMD & Signal & VCC Layer2：GND Layer3：VCC Layer4：GND(Signal/VCC)

When designing, it is necessary to ensure that Layer2 is full GND and minimize power and sensitive signal routing at Bottom Layer (EMI considerations at Bottom Layer).

3.2. Power Supply Network

It is recommended that the 3.3V power supply be routed in the star-shaped mode, as shown in the yellow highlighted part in *__Figure 3-2. Power supply circuit layout design__*. The line of each power Pin is pulled separately from the 3.3V source to the chip Pin, and a large capacitor is placed at the 3.3V source. Copper Plane can also be used at the source. It is recommended that the width of the 3.3V power supply into the module should be 20-30mil. For branches, the width of the PA power Pin (Pin17) should be at least 10mil, and the width of other power pins should be 6-8mil.

If possible, the 3.3V power line is routed at the VCC layer (Layer3). The power line of the TOP layer must be placed in the shield and away from the board edge. The power line and high-speed signal line should not be parallel, and the signal intersection of adjacent layers should be perpendicular. Power lines must be routed through the filter capacitor and then connected to the power Pin, The GND PAD of the capacitor needs to be punched separately (1-2 VIA) to connect to the ground，and all capacitors must not share GND VIA. The GND PAD of the filter capacitor of sensitive pins, such as AVD33_ANA, AVDD33_PA, and AVDD33_CLK, must be drilled separately in the forbidden space of the TOP Layer to the GND Layer 2/3/4 that is laid copper and does not connect to the TOP GND.

Figure 3-2. Power supply circuit layout design
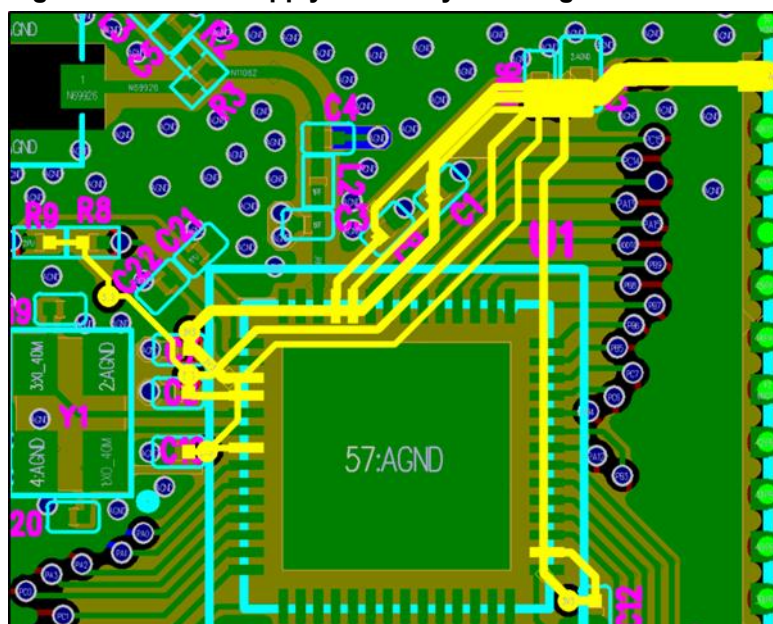

3.3. RF Circuit Design

The RF line impedance must be 50 Ohm. During the design, it is necessary to calculate the line width and line distance of RF routing based on the permittivity of plate and PCB laminated structure, so as to ensure the impedance consistency of RF routing and avoid impedance mutation or offset. Considering the error caused by the process accuracy and other factors in plate making, it is recommended that the RF line width is at least 10mil.

As shown in *__Figure 3-3. RF circuit layout design__*, RF routing should be as short as possible to ensure that the adjacent layer below is a complete GND(no transmission line routing). At the same time, layer penetration should be avoided, and less bending should be done. At the point where bending is needed, the Angle should be greater than 90 degrees and the arc should be pulled; Keep line away from Power lines and high-speed signal lines to avoid strong RF signals coupling to them, which may cause interference to other devices. Place two rows of GND VIA shields on both sides of the line, with the spacing as small as possible.　For some locations where bifurcation is required, a 0R resistor co-lay (R2 and R3 in the figure) can be used.

The third-order π network should be placed as close to the RF Pin as possible and in a "Z" shape. The GND PAD of the RF pin near-end capacitor C3 needs to lead two PAD holes to GND in the cutout area of the TOP layer, add the TOP cutout area so that it is not connected with the TOP GND copper laying. The GND PAD of the far-end capacitor C4 should lead out a short cut line in the cutout area of the TOP Layer and then pass through the hole to GND. The GND Layer (Layer2) should be equipped with the same cutout area (that is, the short cut line refers to the ground of the VCC Layer, and the hole is only connected to the GND copper laying at Layer 3/4).　The total length of the short cut line and the through-hole from TOP to VCC layer should be controlled at about 55mil. Here, the short cut line and the long ground

through-hole can be equivalent to a strong inductor, and the two parallel short ground through-holes can be equivalent to a weak inductor. In this case, the matching circuit structure can be equivalent to (C + L) + L + (C + L). The purpose of the above means is to construct the asymmetry of the matching circuit structure, which can make the second and third harmonics more easily filtered and impedance matching more easily tuned under the premise of using a small ground capacitance, so as to reduce the passband insertion loss of the matching circuit.

Figure 3-3. RF circuit layout design
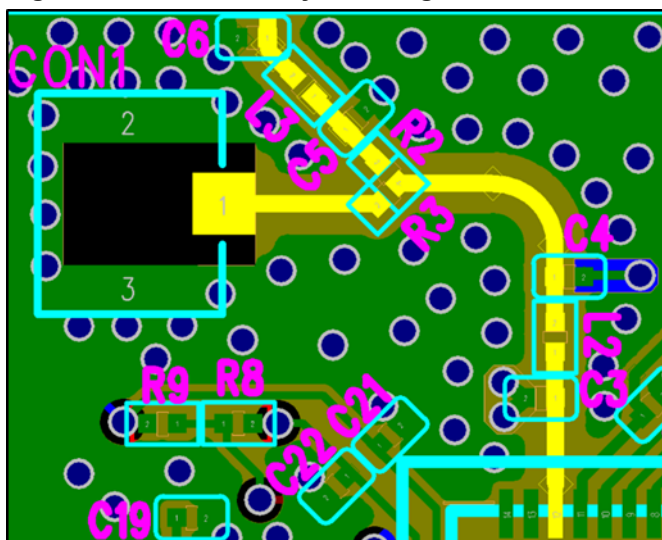
As shown in *Figure 3-4. PCB antenna layout design*，PCB antennas should be placed close to the edge of the board, far away from other transmission lines and devices (especially those transmitting high-frequency signals), and isolated from external circuits by 1-2 GND VIA rows (spacing is as small as possible). In the antenna area, each PCB layer must have polygon pour cutout (that is, no copper is laid). We advise not to expose the Solder mask Top layer of antenna elements (protect the antenna copper skin with coating).

**Figure 3-4. PCB antenna layout design**

3.4.   XTAL Circuit Design

As shown in *Figure 3-5. Crystal circuit layout design*，the crystal should be as close to the chip pin(XI&XO) as possible, far away from magnetic induction devices such as power inductors and radiation devices such as antennas, and isolated from other signals on the same layer by GND laying copper and VIA. Crystal input and output line (XI&XO) width is 6mil, the wire should be as short as possible and less bending, do not cross layer or cross

routing. The load capacitors on both sides are connected to the corresponding GND PAD on the crystal, and multiple GND VIA are placed to improve heat dissipation. Try not to walk any transmission line under the crystal, keep the intact GND laying copper.

Figure 3-5. Crystal circuit layout design
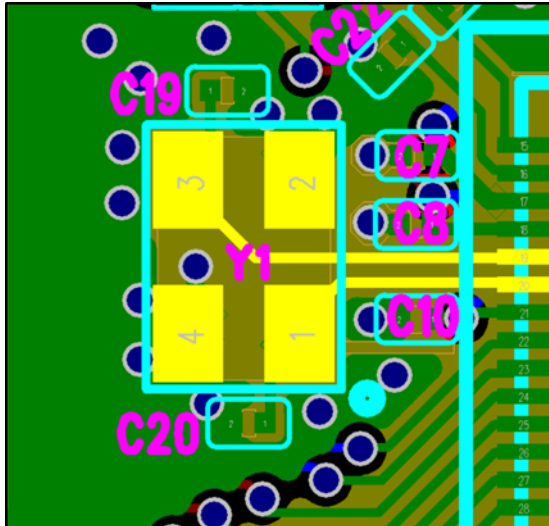
3.5.   GND Integrity & EPAD Design

The Layer2(GND layer) should be a complete GND Plane to ensure that the RF and XTAL parts of the TOP layer are not affected.   At the same time, attention should be paid to the integrity of copper laying on VCC and Bottom GND layer to avoid "island". As shown in _**Figure 3-6. VCC & Bottom layer GND integrity design**_.

Figure 3-6. VCC & Bottom layer GND integrity design
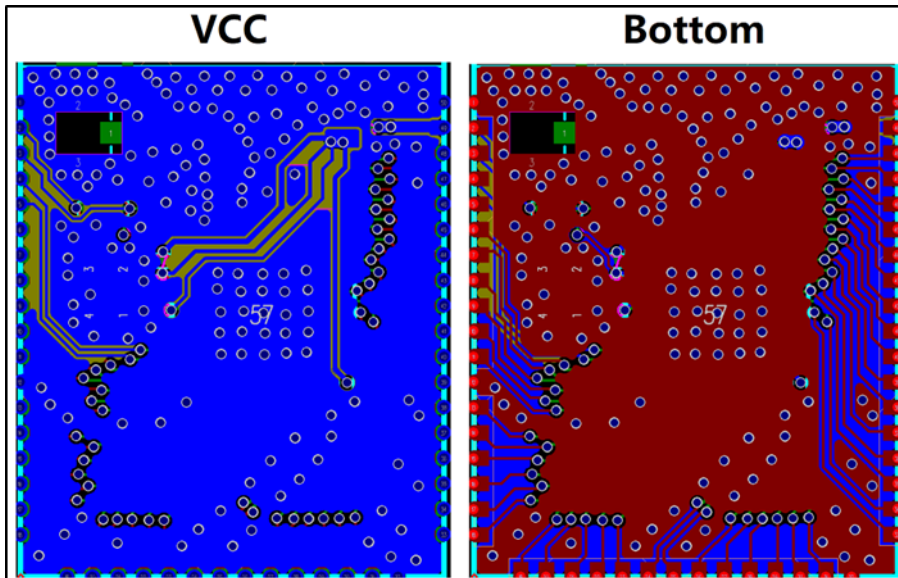
For the chip EPAD, you are advised not to connect it to the external copper layer at the TOP layer.   More GND VIA is used for heat dissipation, as shown in *Figure 3-7. MCU EPAD layout design*.

**Figure 3-7. MCU EPAD layout design**
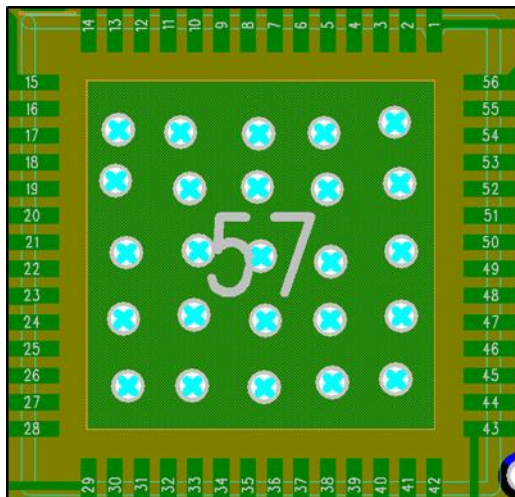
3.6.   Shielding Cover Design

All components and lines in the TOP layer of the module should be confined to the shield frame as far as possible. For lines that need to go through the shield (such as RF lines) in the TOP layer, "escape hole" should be left at the corresponding place of the shield, and other lines should go through the Bottom/VCC layer.

The width of the frame of the shielding cover should be at least 24mil. GND VIA should be placed on the frame pad.   At least 15&10mil between shielding cover and edge pad and routing; The height of the shield is determined by the height of the components, and the influence of the shield height should also be considered when designing the antenna. The reference design of the shield pad is shown in the yellow highlighted part of *Figure 3-8. Layout design of shielding cover*.

Figure 3-8. Layout design of shielding cover
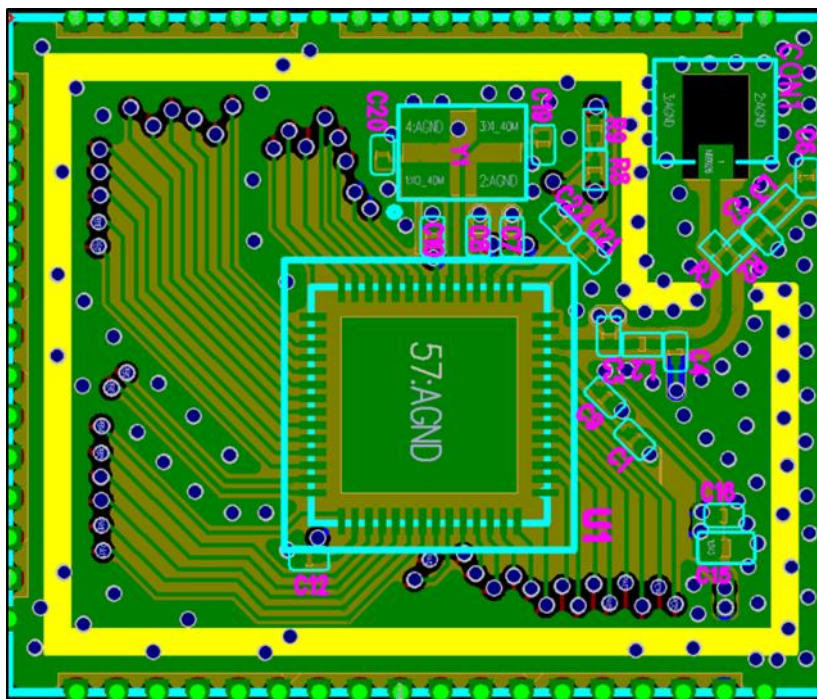
3.7.   Routing and Ploygon Design

In addition to the power line and RF line width requirements described above, it is recommended that the GPIO line width should be 5-6mil and the GND line width should be at least 8-10mil. The width and distance of USB differential pair lines should be selected according to the impedance simulation results. The differential pair should be of equal length and equal spacing. The lines and components should be symmetrical, and the lines should be as short as possible. The adjacent layer below should be kept intact for GND, and the TOP layer should be isolated from other lines using GND VIA. As shown in **_Figure 3-9. Differential pair routing layout design._**

Figure 3-9. Differential pair routing layout design
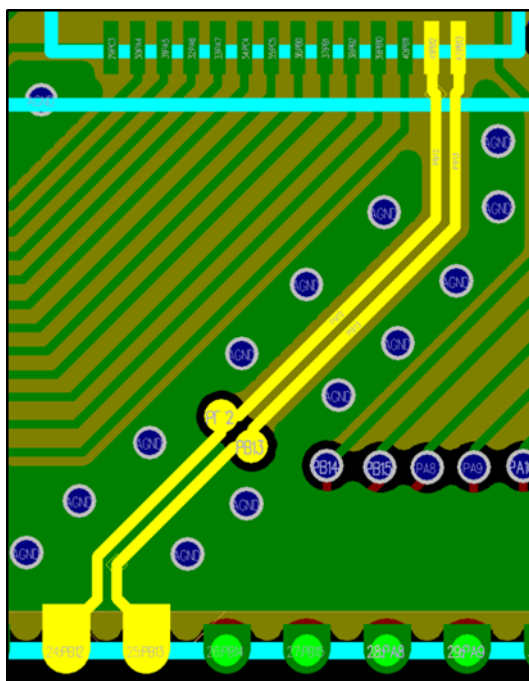
The copper laying area of the module PCB should be close to the size of the board frame. Before laying copper, you can first hit more GND VIA in the blank area according to irregular ways, and hit a row of GND VIA on the side of the board; Each component GND PAD is placed close to the VIA; To avoid islands, copper will not be laid in the area where GND VIA cannot be placed due to space limitations.

4. Package Description

GD32W515 series has two package forms, QFN56 and QFN36 respectively.

Table 4-1. Package Model Description

Part Number	Package
GD32W515PxQ6	QFN56(7x7, 0.4pitch)
GD32W515TxQ6	QFN36(5x5, 0.4pitch)

(The unit of size is mm)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Nov.30 2021

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